Regional Summit 2008 NAFEMS

2020 Vision of Engineering Analysis and Simulation

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Issues Facing Engineering Simulation: A CAE Providers Perspective

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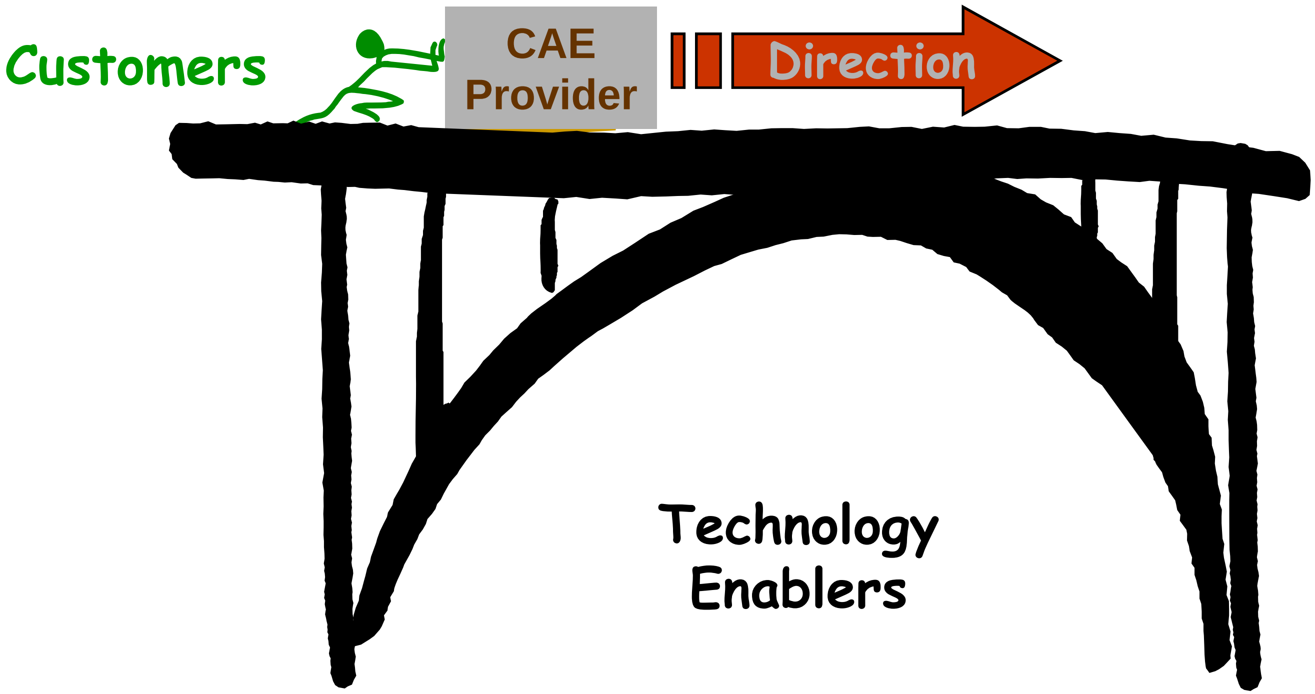
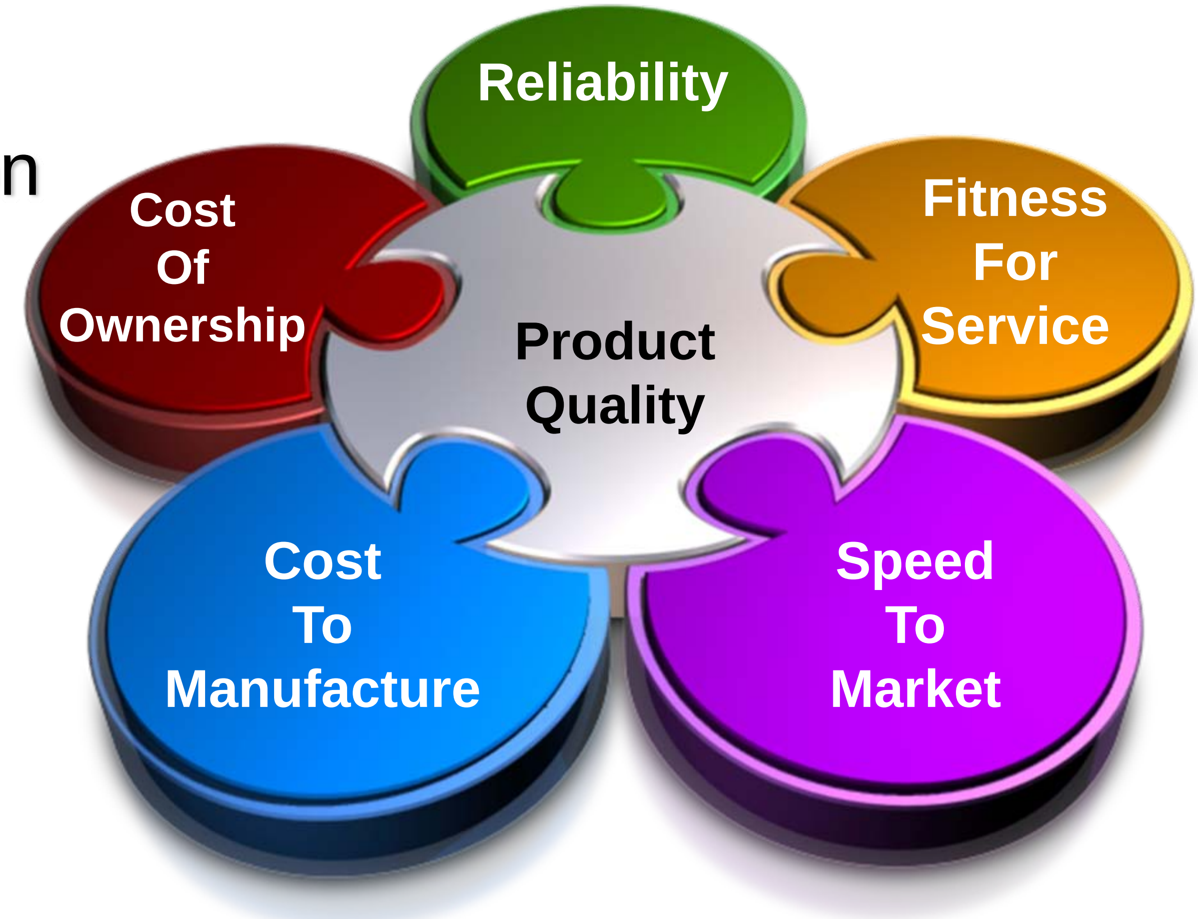
Agenda

- Customer drivers
- Technology enablers
- CAE directions and issues



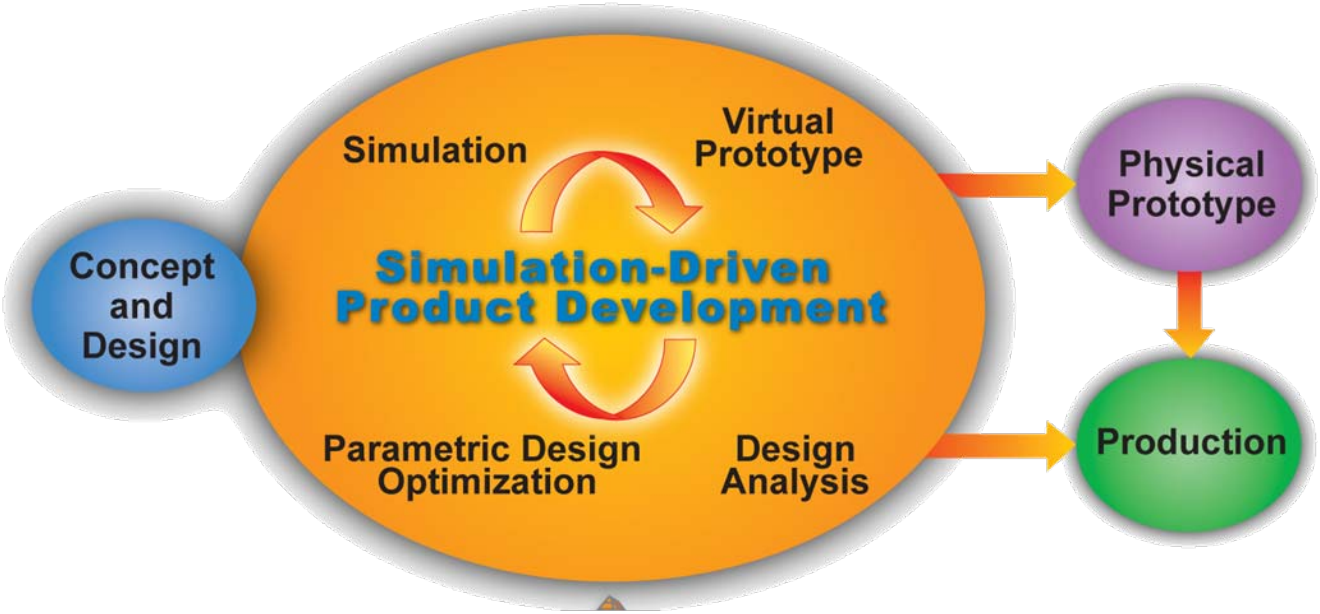
Customer Drivers

- Upfront analysis
- Variability
- System simulation
- Model fidelity
- Multiple physics



Upfront Analysis

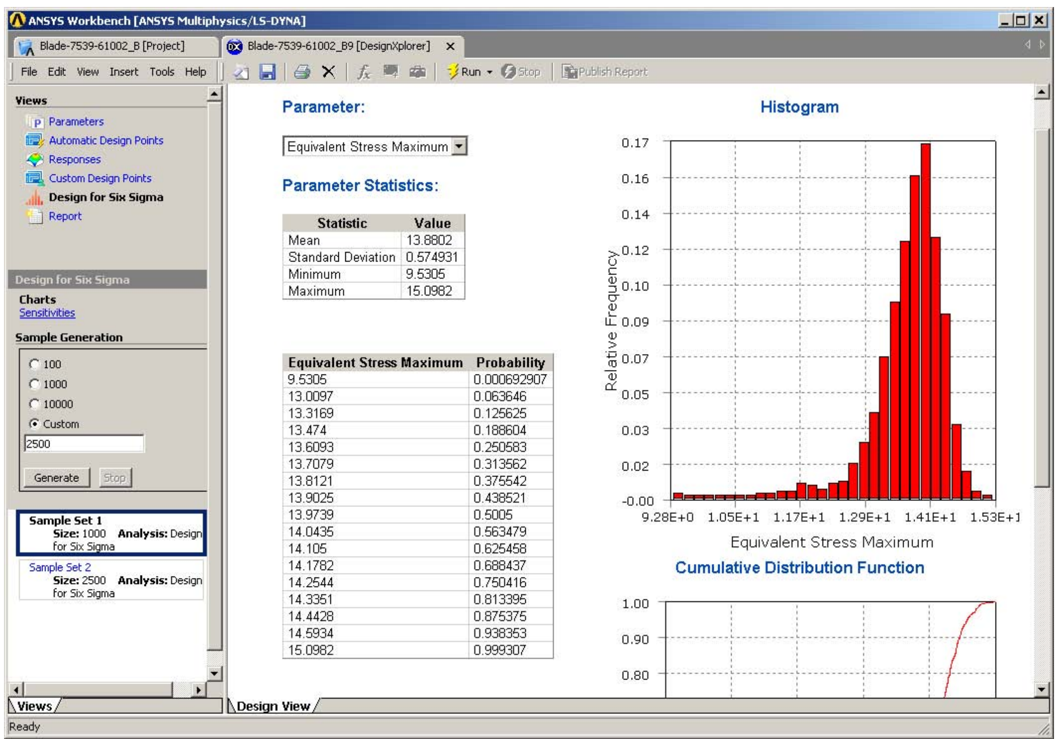
- Simulation-Driven Product Development (SDPD)

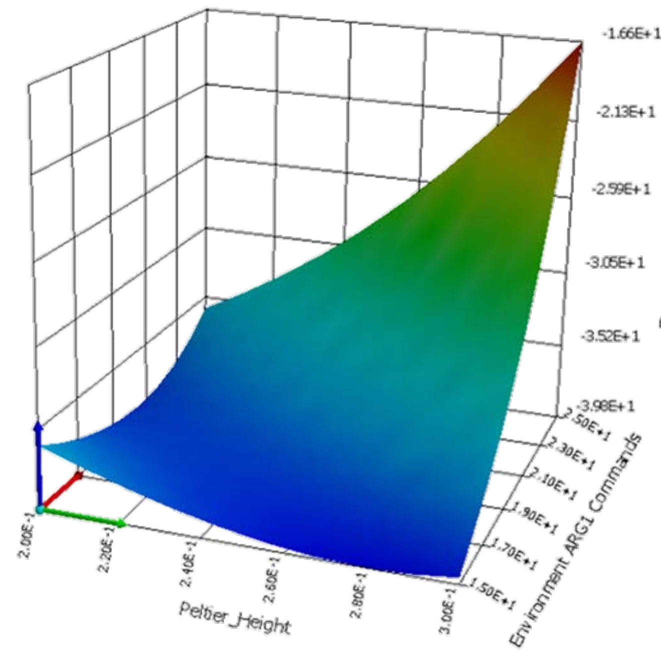


Use simulation to impact design early on when design changes are relatively inexpensive

Variability

- Design of experiments (DOE)
- Design for six sigma (DFSS)

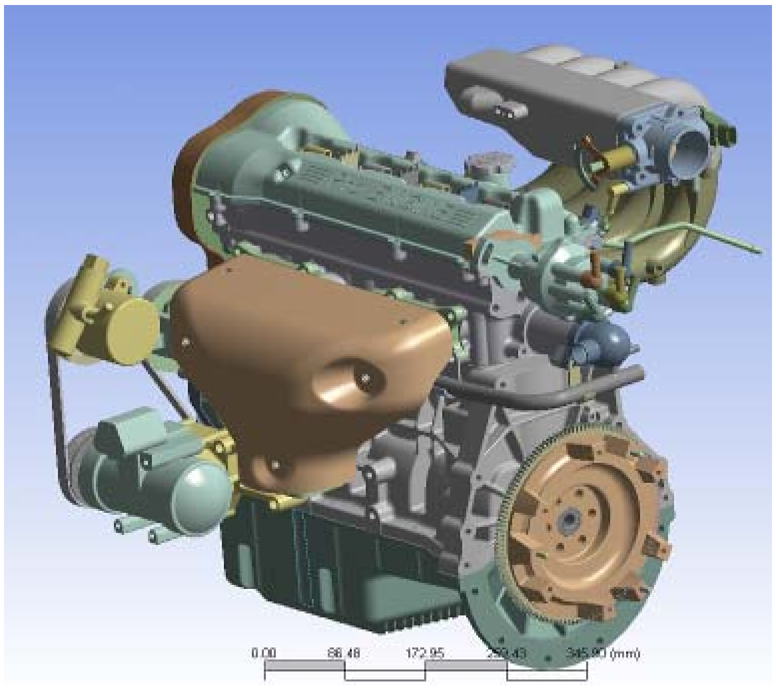


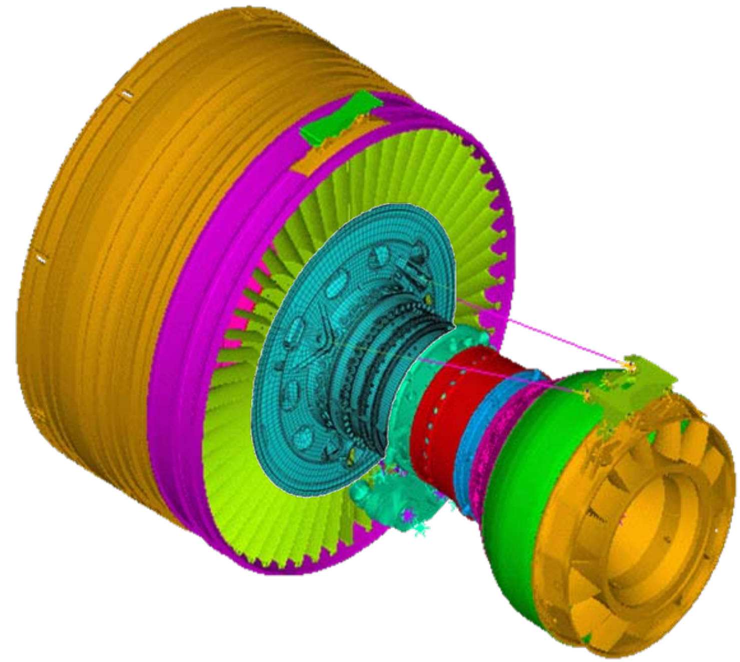


Simulation allows for quick “what if” iterations and to understand the design space and build in robustness

System Simulation

- Entire assemblies

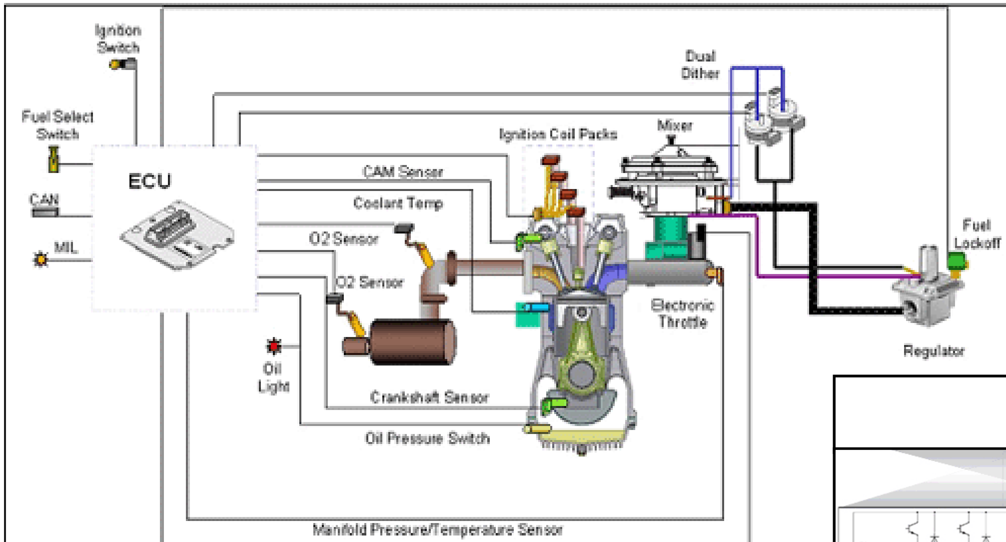


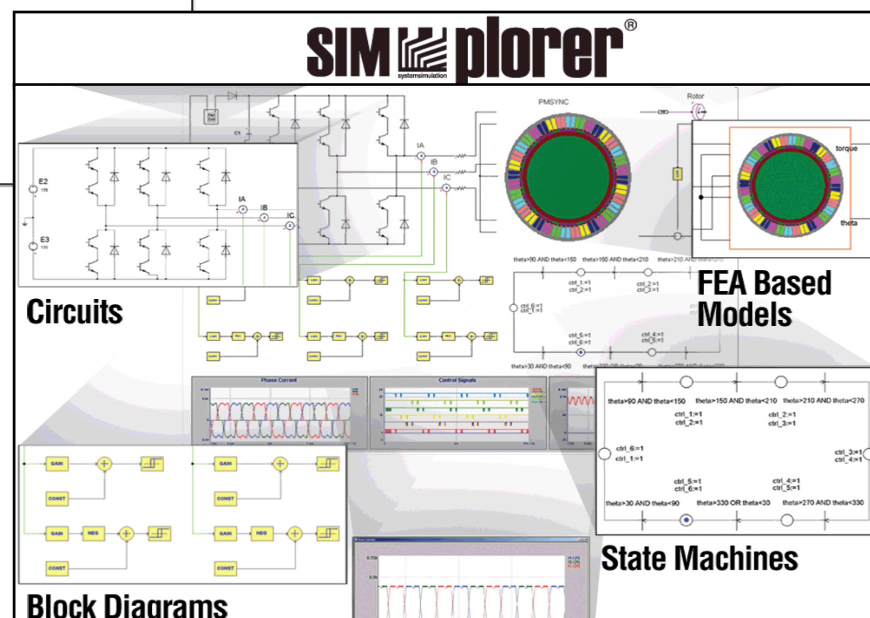


Optimize the whole product, not each component individually and remove assumptions on part interactions

System Simulation

- System modeling

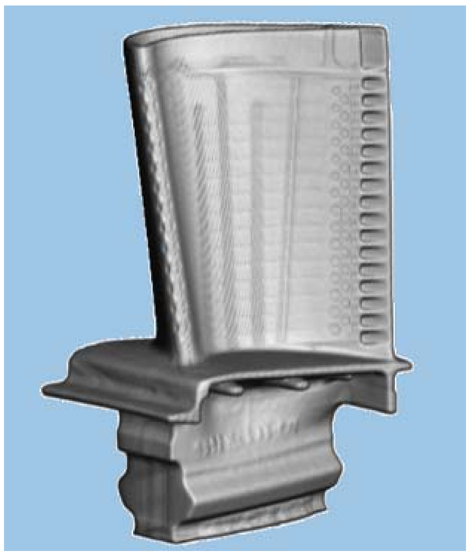




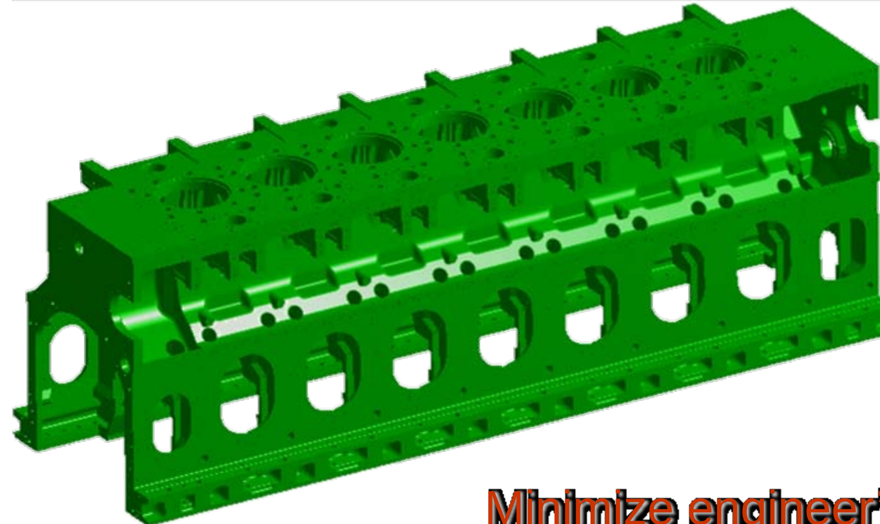
Mechatronics: simulate the entire system behavior

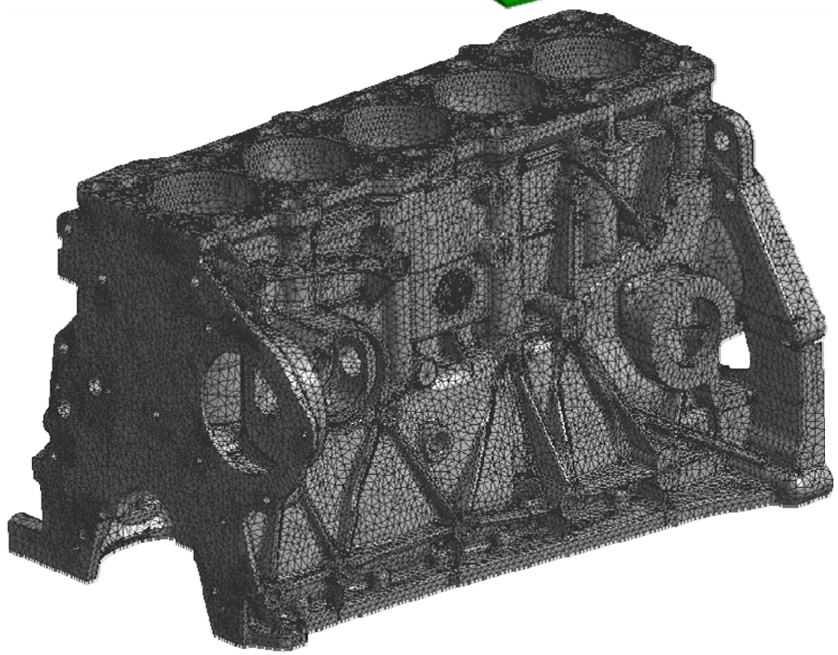
Model Fidelity

- Hot spots
- Geometry defeaturing



Where will fatigue failure occur?

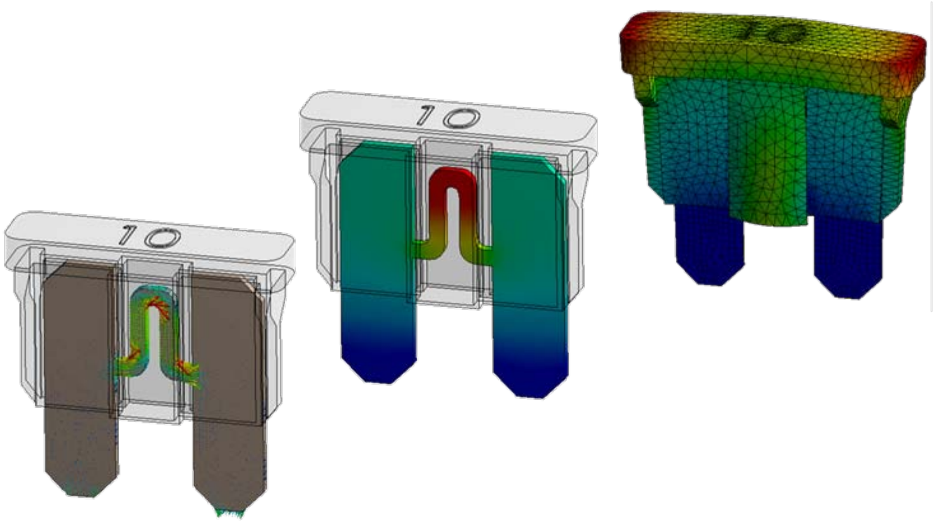




Minimize engineer's time in creating the mesh

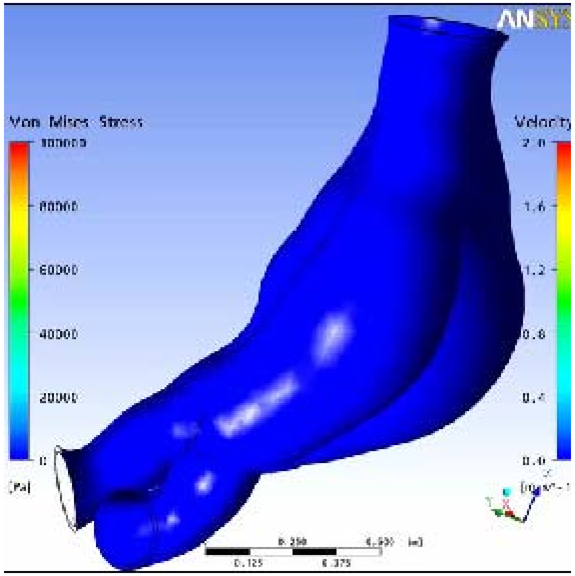
Multiple Physics

- Include all relevant physics



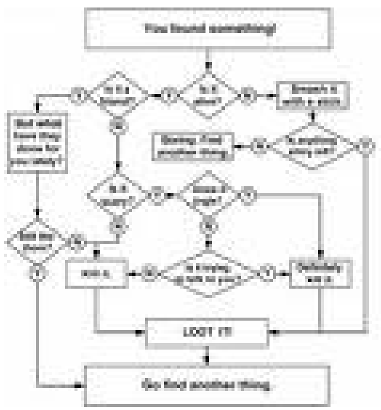
Electric-thermal-structural

Fluid-structure interaction

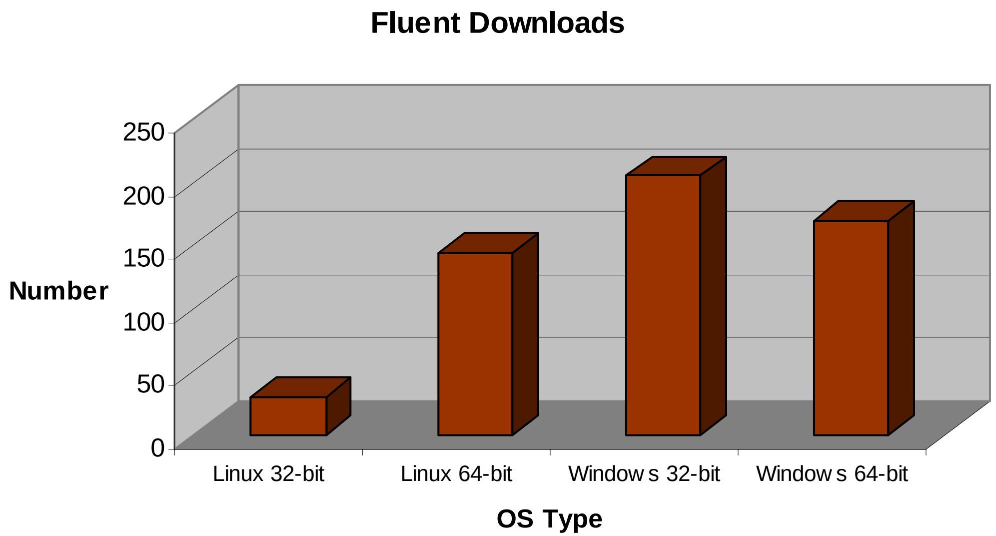


Technology Enablers

- Ubiquitous 64-bit computing
- Multi-core
- Algorithmic advances



Ubiquitous 64-bit Computing

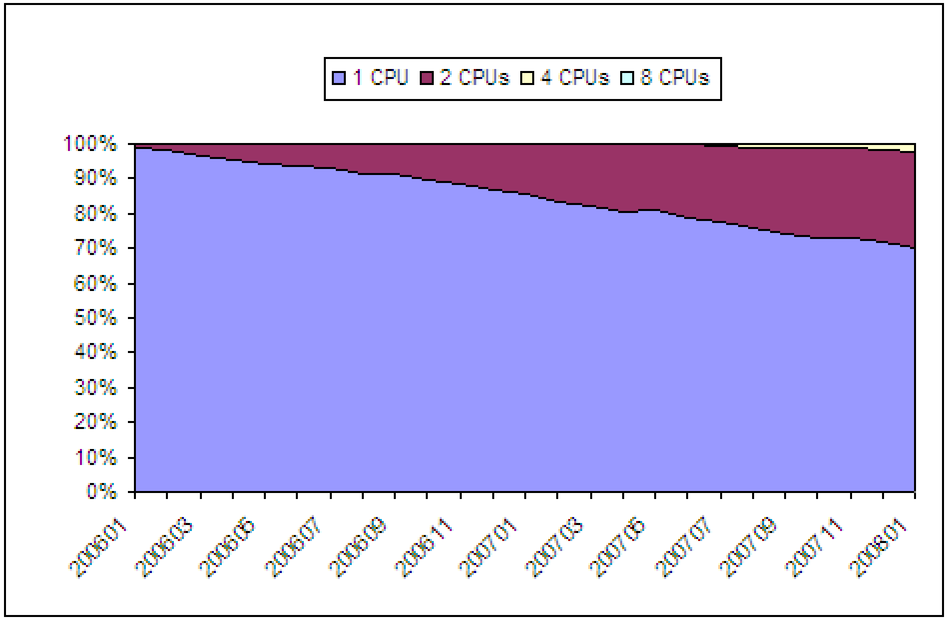


The engineers desktop is quickly migrating to 64-bit!

➨ 64-bit means 8, 16, 32 GB memory on the desktop

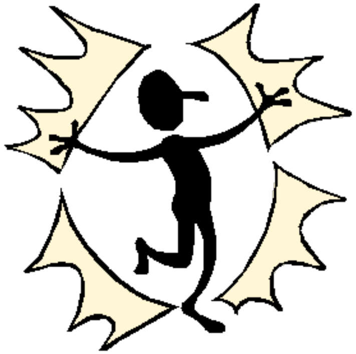
Multi-Core

- 10s to 100s of cores coming on the desktop
- 80-core chip in research stage
- …GPU's as "multi-cores" too!



Multi-Core Trends (Home/Business PCs)
http://www.pcpitstop.com/research/

Algorithmic Advances



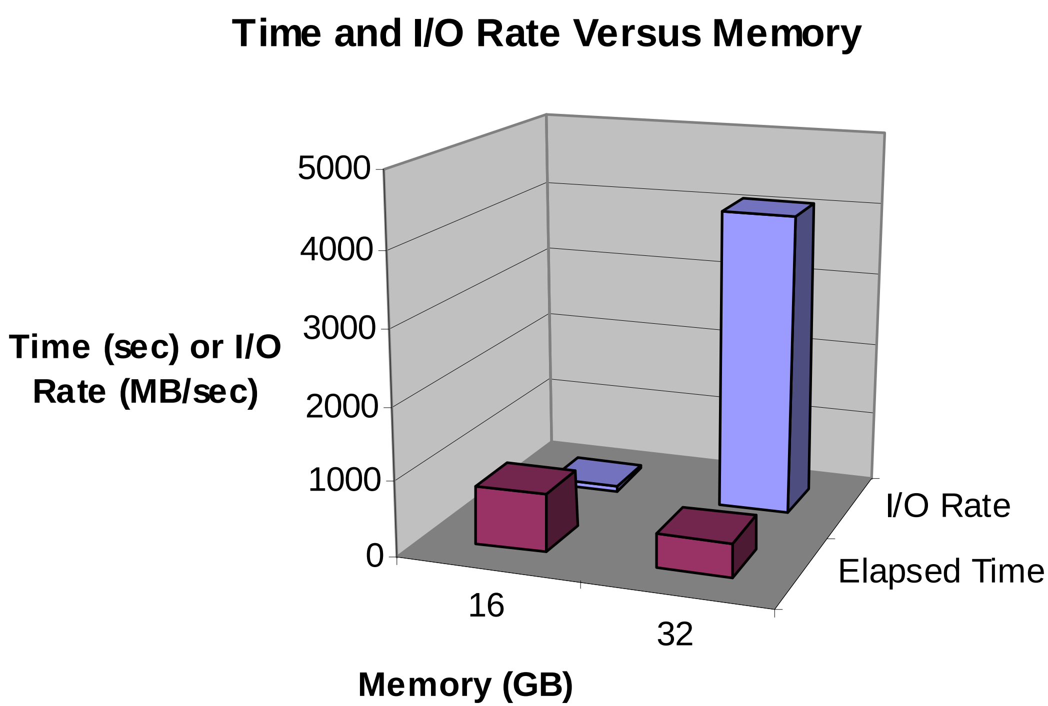
- Parallel Programming
  - Shared memory (OpenMP)
  - Distributed memory, e.g. clusters (MPI)
- Sparse solvers
  - Left-/right-/combined-looking supernode techniques
  - Dynamic balancing
  - Hybrid parallelism
- Iterative solvers
  - Scalable domain decomposition methods

CAE Directions and Issues

- Embrace large memory
- Pervasive parallelization
- Reduced order modeling

Embrace Large Memory

- What can we do with gigabytes of memory?
  - In-core algorithms, e.g. sparse solver
  - Use it to buffer I/O



Embrace Large Memory

- Issues
  - Memory bus speeds lagging “can’t feed the cores fast enough”
  - Cache-friendly algorithms
  - Multi-core memory affinity

Pervasive Parallelization

- Everything must be parallel!
- Issues
  - Algorithmic
  - Multi-core

Amdahl's Law

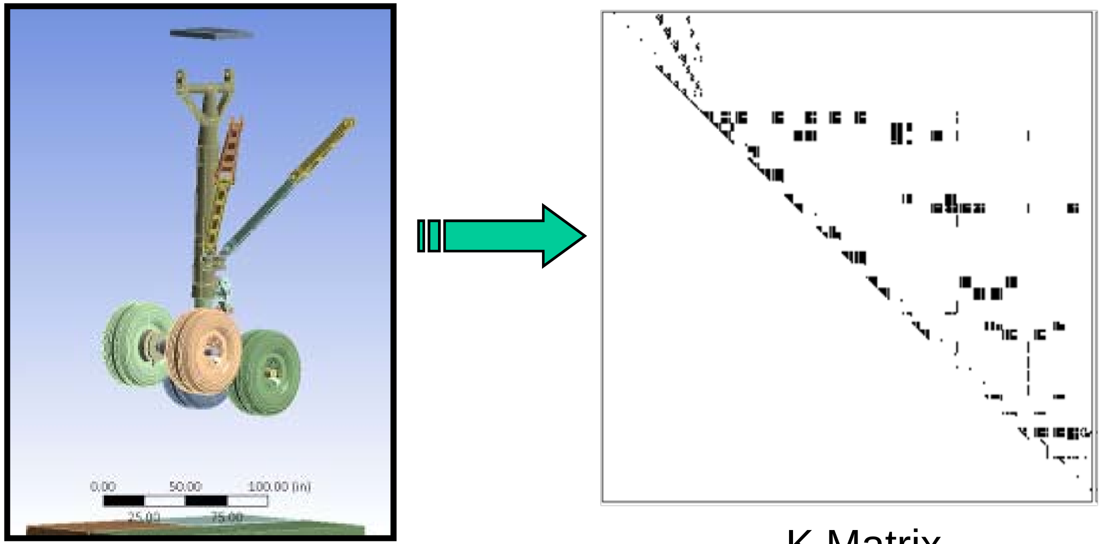
Speedup = $$\frac{1}{F + (1 - F)/N}$$

If only 10% of the code remains serial, the most speedup you can get is a factor of 10!

Algorithmic Issues

- Everything can't be parallel…
- Equation solver issues
  – Global constraints (MPC's)
  – Lagrange Multipliers

These cause scalability problems due to their global nature!: G^TKG

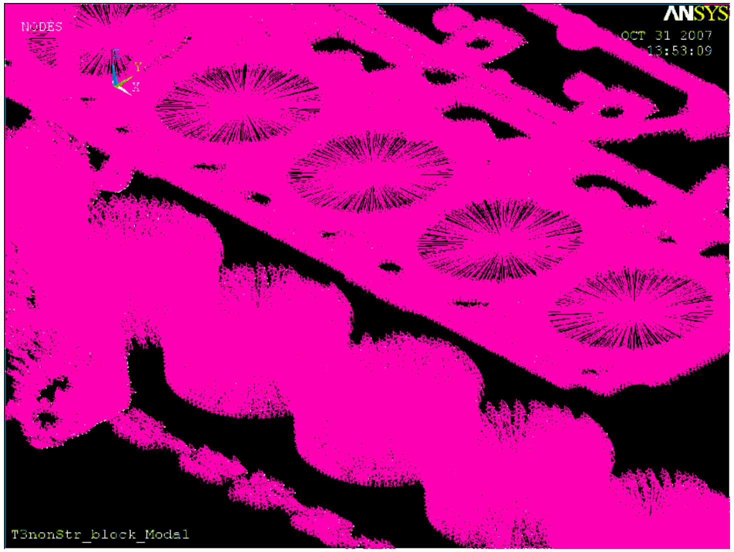


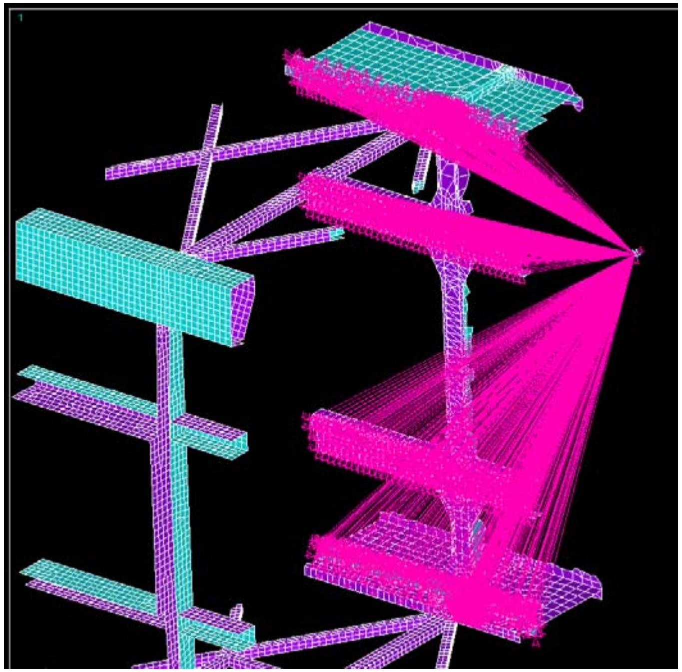
K Matrix

We're not solving FE equations anymore!

Algorithmic Issues

- Equation solver issues (cont)
  - Global constraints (MPC's)



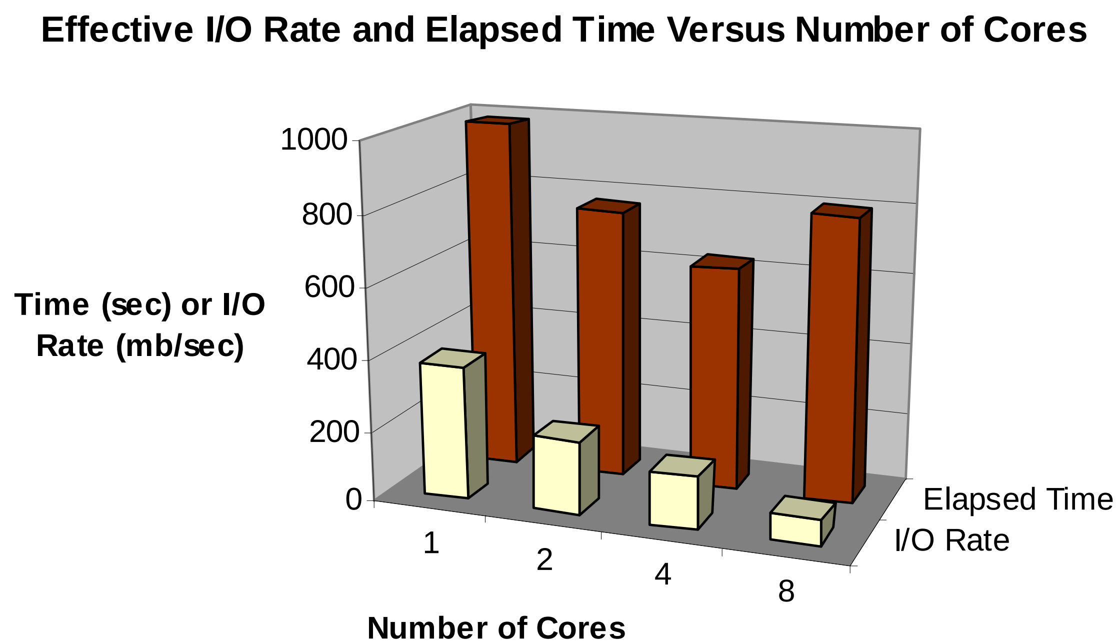


The number of MPCs can be on the order of magnitude of the number of elements!

Multi-Core Issues

Just when we were mastering clusters…

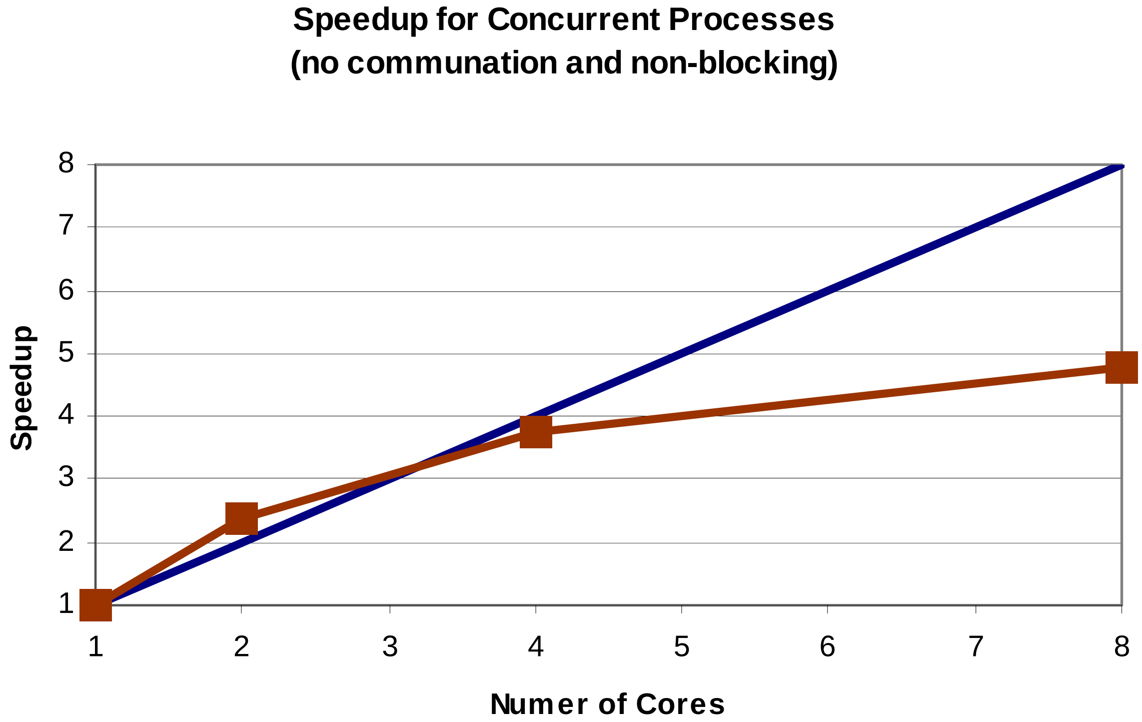
- I/O *not* scalable



Minimize I/O or use large memory to buffer it!

Multi-Core Issues

- Multi-core architecture *not* perfectly scalable



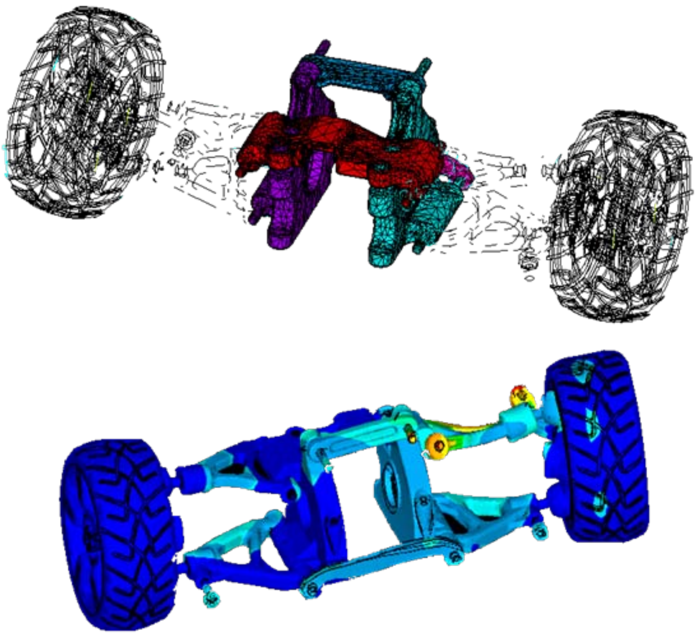
Run 2 jobs simultaneously or back-to-back with 2 processors?

Reduced Order Modeling

- Emerging area for dealing with large models and system models
- Techniques
  - Substructuring/superelements (SE) for statics and Component Mode Synthesis (CMS) for dynamics
  - Automated Multi-Level Substructuring (AMLS) for modal and harmonic (frequency) regime
  - Variational Technology (VT) for automated ROM

Traditional CMS/SE

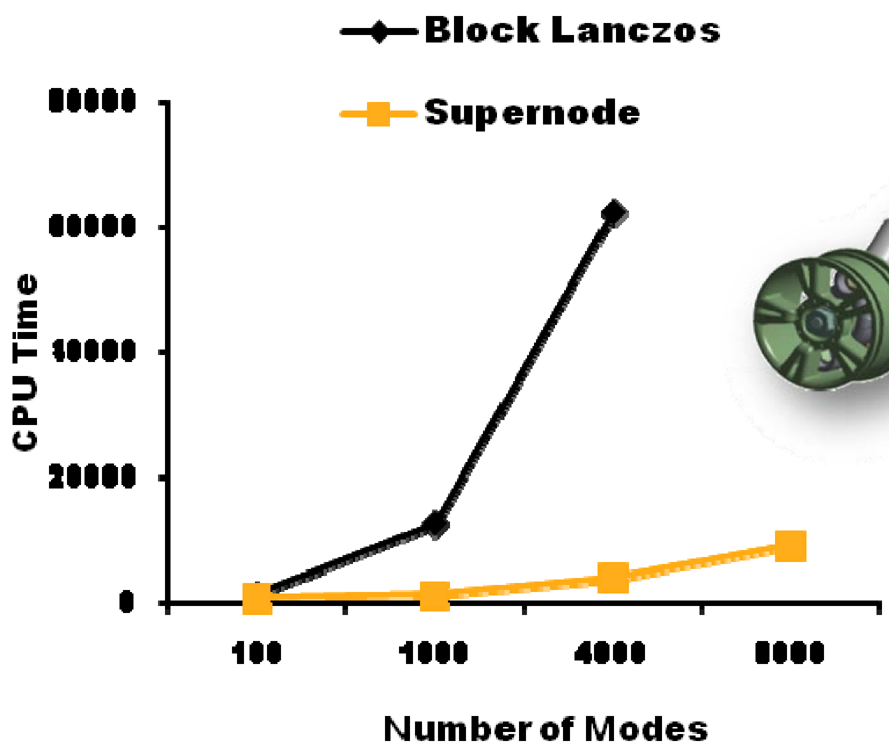
- CMS (Superelements) traditionally used for reduced-order modeling

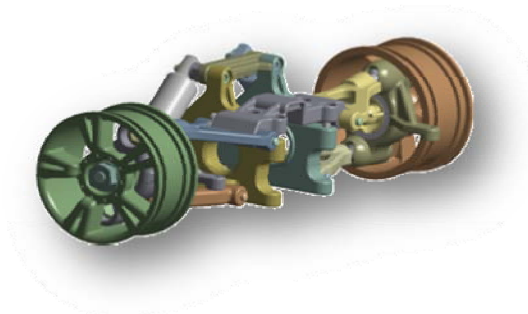


Matrix reduction is expensive – CPU and disk space

AMLS

- Automatic division of a model into 1000s of CMS substructures (or supernodes)

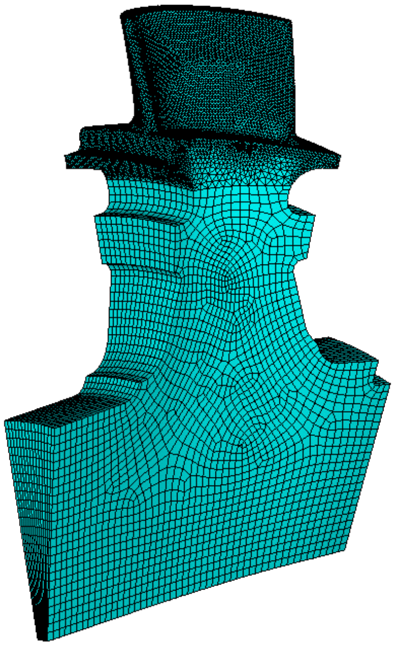




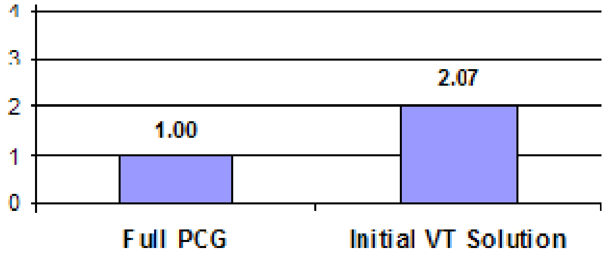
Very fast for high modal density problems

Variational Technology (VT)

- Build subspace (Krylov vectors) on the fly during a transient or nonlinear analysis



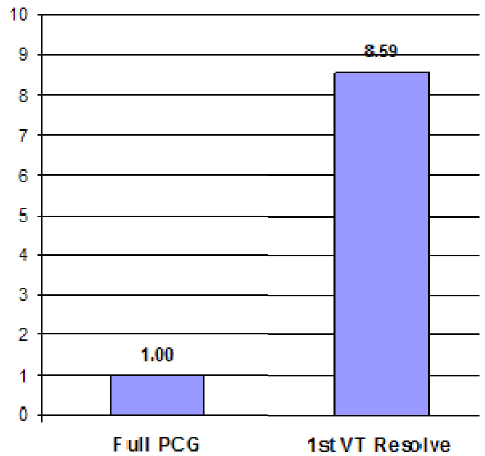
Thermal transient



Relative Speedup

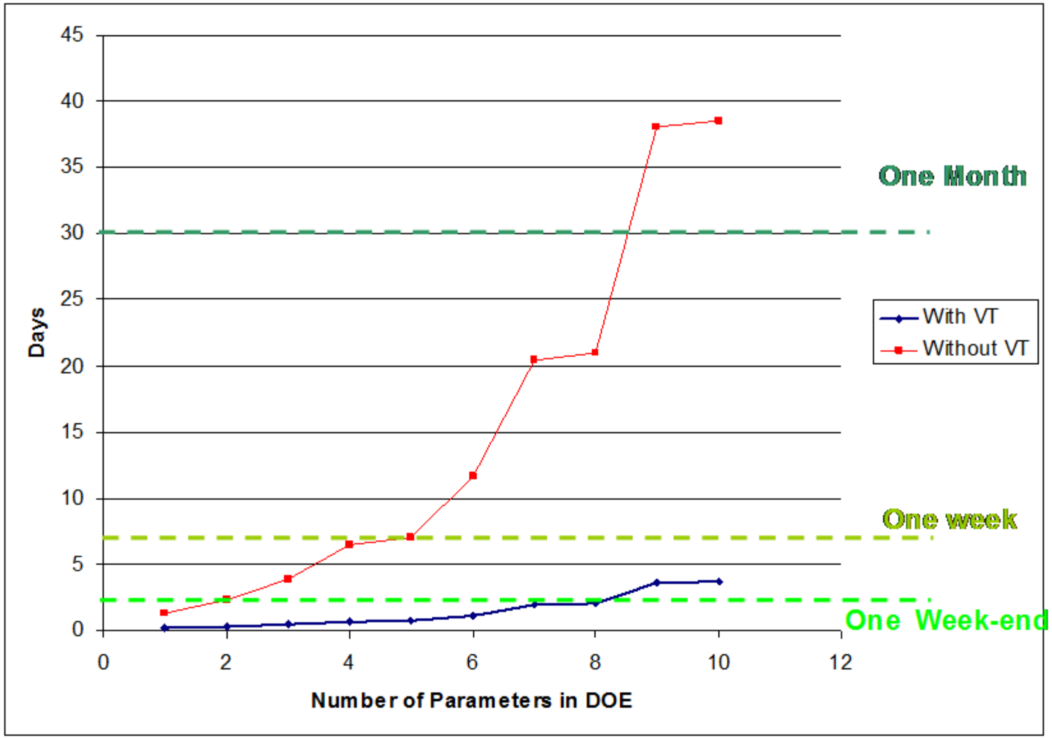
Used to accelerate subsequent time-step solutions

VT



Relative Speedup for 1 Parameter Change

Used to quickly find solutions due to parameter changes

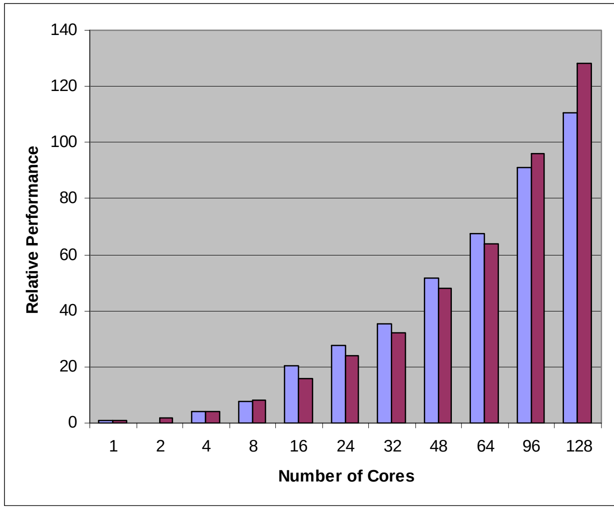


Time for Multiple DOE Parameter Changes

Future CAE Challenges

- Effective use of 1000’s of cores in a single box: code parallelization, memory, I/O
- Robust and scalable solvers for the multi-core environment (for implicit structural FEA codes)
- Handling of the immense amount of data (spatially and temporally) being produced

Solver scalability of our CFD brethren

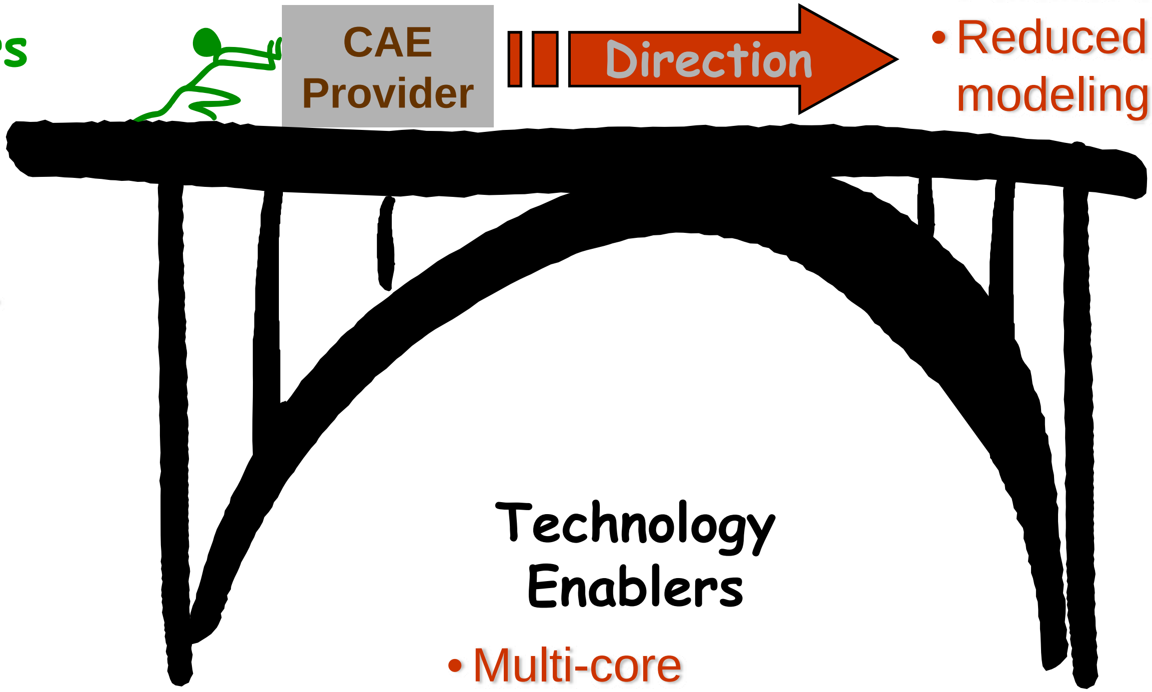


Summary

- Use the available memory
- Parallel everywhere
- Reduced order modeling

Customers

- Larger models
- Multiple physics
- Assemblies
- System behavior



- Multi-core
- Large memory
- Parallel algorithms

Thank You!

- Questions?

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