MODELING AND SIMULTION OF SEMICONDUCTOR PROCESSING REACTORS

Umesh Kelkar

umesh_kelkar@amat.com

Applied Materials, Inc

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ABSTRACT

Semiconductors are at the heart of the explosive growth seen over the past decade in mobile devices. The complexity of the semiconductor processing hardware and processes has significantly increased to meet the ever increasing demands for miniaturized, high performance and low power consumption semiconductor chips. A modern semiconductor processing reactor has highly complex multi-physics environment to deposit or etch materials in submicron features. The author would discuss the importance of coupled physics modeling and simulation involving heat and mass transfer, gas dynamics, electromagnetics, plasmas, gas phase and surface chemistry. The disparate length and time scales necessary to model highly coupled physics in these reactors make truly CAE driven development of semiconductor processing reactors very challenging. However, CAE has played a vital role in process and hardware development over the years to expedite the product development and reduce cost and time. Several examples pertaining to various reactors used in semiconductor processing will be presented.

Thermal, magneto-static, plasma, and feature level modeling of PVD system has enabled extendibility of this technology over several generations. CAE is effectively used to design critical architectural elements (sputtering target, shield, electrostatic chuck etc) of the system as well as to guide the process development. Flow, thermal, chemistry modeling of silicon epitaxial deposition system will be presented to demonstrate the value of CAE in design and development. Specifically, the results from the gas inject optimization in a cross-flow reactor to obtain uniform film deposition across a 300mm wafer will be presented. In addition to the reactor level modelling, several feature level modelling examples will be presented.