WHITE PAPER

Electrothermal Mechanical Stress Reference Design Flow for Printed Circuit Boards and Electronic Packages

This paper presents a reference design flow for solving the electrical, thermal and mechanical challenges of a printed circuit board (PCB) using simulation tools from Ansys. This approach can be utilized for all electrical CAD (ECAD) types such as IC packages, touch panel displays, and glass and silicon interposers. The authors followed this reference design flow for analyzing a PCB virtual prototype used in the consumer electronics industry. The design flow details nearly all aspects of the modeling technique from studying electrical connections in a schematic and setting up the PCB to analyzing the electrical, thermal and mechanical characteristics of the board — all using Ansys tools. The multiphysics simulation yields power losses across the entire board and its objects, determines whether the integrated circuit (IC) and overall board temperatures lie within safe operating limits and predicts overall PCB reliability, taking into account all its components and heat sinks.

Aligned with this paper is a collection of YouTube training videos on the Ansys Electronics Channel that demonstrate in detail all the steps for performing the electrothermal and structural analyses of a modern PCB from the consumer electronics industry. The videos are available under the playlist:

Ansys Electronics: Electrothermal Mechanical Stress Reference Design Flow for Printed Circuit Boards and Electronic Packages

If you follow our reference design flow, you can:

1. Translate ECAD geometry to Ansys solutions
2. Review schematics
3. Analyze power integrity and DCIR in Ansys SIwave
4. Perform automated and iterative thermal analysis
5. Perform temperature post-processing in Ansys Icepak
6. Generate temperature profiles for the board in Icepak
7. Prepare a PCB for use in Ansys Mechanical
8. Assemble the project in Ansys Workbench
9. Import layer metallization on the board using the “Trace Mapping Technique”
10. Transfer temperatures from Icepak to the board in Mechanical
11. Simulate the board for thermal stress, deformation and elastic strain.

The multiphysics analyses also let you build “what-if” scenarios where you can make modifications to your design. For example, you can determine mitigation measures to minimize power losses and study cooling techniques (like adding heat sinks) to ensure board and IC temperatures are safe to operate. The “what-if” tests also let you try out different material properties for minimizing thermal stress.

This comprehensive reference design flow will give you a general guideline for performing electrothermal and structural analysis for *any* printed circuit board or ECAD.

Motivation for Electrothermal and Structural Reliability

A PCB is composed of successive layers of different materials laminated together.

Prepreg and inner layer cores are sandwiched between copper layers with varying thicknesses. The PCB forms the base to mechanically support and electrically connect the components that are mounted on it. Considering the structural composition of a PCB with mismatched coefficients of thermal expansion (CTEs) for the different materials, mechanical and electrical difficulties are typical for a PCB.

PCB problems can be broadly classified as electrical, thermal and mechanical. Electrical problems include signal integrity, crosstalk and electromagnetic interference. Current flow in a PCB and through the electronic components causes power losses across the board and leads to power dissipation in the

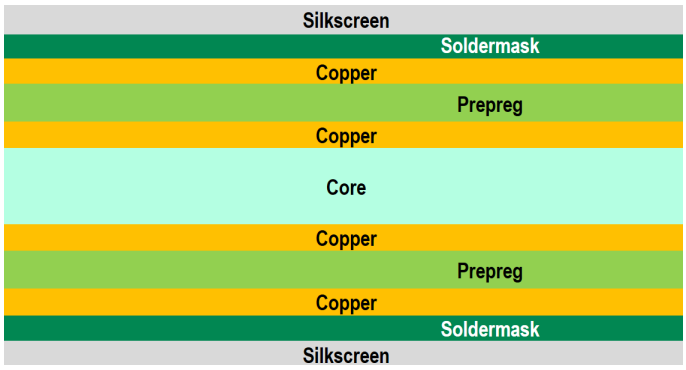

Figure 1. PCB fabrication view

components, mainly the ICs. Power losses in conductors within the board and heat generated by ICs increase their temperatures, leading to thermal problems. Moreover, modern microprocessors can demand peak currents of 100 amperes or more. These high currents cause significant heat dissipation in the ICs and significant Joule or Ohmic heating in the connected power planes and traces.

Even a small change in temperature can affect a device's performance due to the inverse relationship between electrical and thermal conductivities. Temperature gradients across the board and components can produce mechanical reliability problems owing to the cyclic nature of thermal transients. This follows from the principle of the bimetallic strip, which can convert temperature differences into mechanical displacement. Per this principle, when two metals with dissimilar CTEs are bonded together, they will bend if they are heated. Because a PCB is made up of many layers of different materials laminated together, it can bend when heated. This bending can cause solder joints to crack or even result in delamination of the board or traces on the PCB.

Electrothermal Mechanical Stress Solutions from Ansys

These electrical, thermal and mechanical challenges become significantly worse as the board complexity increases. Therefore, it is critical to use simulation tools to identify potential failure points prior to fabrication and perform "what-if" tests to mitigate these problems early in the design cycle.

Ansys provides time-tested simulation tools for solving any physics from electromagnetics, computational fluid dynamics or mechanical engineering. Specific challenges impacting performance and PCB reliability are power integrity, signal integrity, electromagnetic interference, vibration, thermal transients and stress. Ansys has developed a unique Chip-Package-System (CPS) electrothermal mechanical stress reference design flow to detect these problems early in the design cycle. The solution is comprehensive, carefully examining the interaction between the chip, package and system from standpoints of electrical issues and thermal stress in an integrated environment.

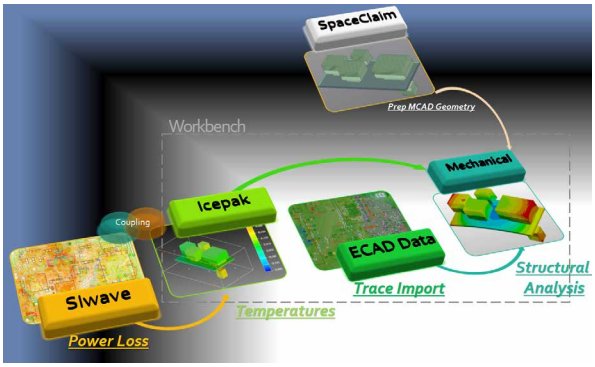

Figure 2. Pictorial depiction of reference design flow

Products used to analyze electrothermal and structural problems are as follows:

- Ansys SIwave
- Ansys Icepak
- Ansys Mechanical Enterprise (which includes Ansys SpaceClaim Direct Modeler)

Simulation Tools from Ansys

This section gives a brief description of Ansys products and the role each of them plays in the flow.

Ansys SIwave

SIwave is a specialized tool that allows users to import electrical CAD (ECAD) data to predict electrical behavior and performance. In SIwave you can predict signal integrity, power integrity and DC voltage drop performance along with EMI/EMC and various other analyses. In the electrothermal stress problem, SIwave is used for running a DCIR analysis to calculate the DC power losses across the ICs and PCB.

Ansys Icepak

Icepak performs computational fluid dynamics analyses for IC packages, PCBs and electronic assemblies from chip level to data centers. Icepak predicts steady-state and thermal transient temperatures for heat transfer mechanisms such as conduction, radiation, forced air and natural convection. For our problem, Icepak calculates temperatures across the board and ICs while predicting whether components are within safe operating temperature limits. Icepak has forced convection and natural convection thermal analyses options for the board and its components. In forced convection, you can model air flow analysis with fans and specify the speed and direction of the air flow. In natural convection, the distribution of heat across the board is used to determine the air flow.

Ansys Mechanical Enterprise

Mechanical solves complex structural engineering problems. In our problem, Mechanical calculates the thermal stress, deformation and elastic strain of the board.

Ansys SpaceClaim Direct Modeler

SpaceClaim Direct Modeler (SCDM) is a 3-D MCAD modeling software package used to create, edit and repair geometry. SCDM is included with the Ansys Mechanical Enterprise product. The PCB for our problem is imported into SCDM with the corresponding heat sinks. Essentially, SCDM acts as a bridge between ECAD, SIwave and Mechanical.

Ansys Workbench

Workbench is a platform that integrates applications using common and compatible data models for multiphysics problems. In the multiphysics problem of our PCB, Workbench helps to link thermal simulation results from Icepak to Mechanical. Also, ECAD data is mapped onto the board geometry in Mechanical through Workbench.

The reference design flow is described in the following sections.

/ Stage 1: Translate ECAD Geometry to Ansys

The first stage of our multiphysics simulation is to translate the ECAD geometries from third party vendors into Ansys tools, particularly, SIwave. ECAD geometries for packages and PCBs are created in various layout tools. Ansys actively supports ECAD translations from the vendors shown in Figure 3.

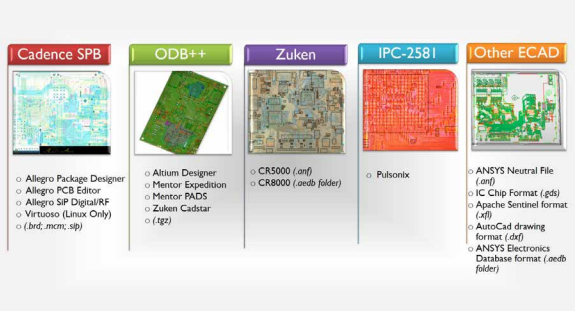

Figure 3. Supported ECAD translations

From these third party layout tools, complete designs with arbitrary power and ground planes, vias, signal traces, wirebonds and circuit elements can be translated with unprecedented accuracy and speed into SIwave. Depending upon the type of layout tool, there are different options available for easy translation of ECAD geometries to SIwave. Ansys products offer a lot of flexibility in this regard.

For example, you can very quickly generate an Ansys equivalent model from Cadence SPB by "dragging & dropping" the associated file (.brd, .mcm or .sip) into the SIwave interface, assuming Cadence is installed on the same machine as SIwave.

Alternatively, if you install Layout Integrations for ECAD, which is a separate installation option within the Ansys Electromagnetics Suite download, it adds Ansys menu items within Cadence SPB products. Through this Ansys menu, you can create .anf and .cmp files or launch HFSS and SIwave directly from within the Cadence environment.

In this paper we illustrate the analysis flow using a printed circuit board that was originally created in Altium Designer. Altium Designer exports the design in ODB++ format. This ODB++ directory is imported into Ansys SIwave. Design automation features in SIwave let you import ECAD files from many popular layout tools as shown in Figure 3. The translator binaries that come with the Ansys EM Suite installation extract a complete list of nets from the ODB++ database easily. The full board with its layers, material properties, components, VRMs, ICs (microprocessors, FPGA, DDR2 RAM), vias and traces are all accurately translated to SIwave. Figure 4 shows the virtual prototype of the PCB in Altium Designer and the accurately translated version of the same prototype in Ansys SIwave. Reference designators are labeled for your ready reference. In its physical form, this printed circuit board is used in electronic devices for multimedia applications.

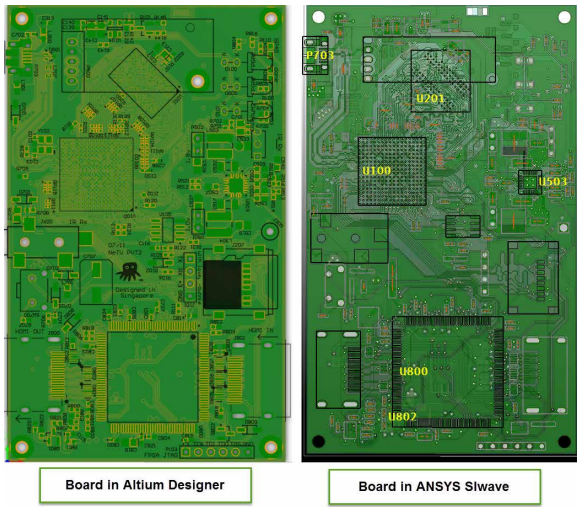

Figure 4. PCB translated from Altium Designer to Ansys SIwave

Note: To learn how to translate ECAD geometries to Ansys watch the YouTube Videos available under the playlist Ansys Electronics: Translating ECAD Databases into Ansys.

Stage 2: Schematic Review

Reviewing a schematic and understanding how it works involve recognizing the key components, ICs and electrical connections. This will help you comprehend how to set up the power sources and sinks within SIwave. Divide the schematic into functional blocks and identify components such as microprocessors, voltage regulators and sensors that generally do the most work on a circuit. Also, follow the nets, and find the corresponding pins and electrical connections. To illustrate, see a portion of the schematic shown in Figure 5. On our board, there are six power nets and two ground nets. These six power nets are P1.0V, P1.2V, P1.8V, P1.8VA, P3.3V and P5.0V. The two ground nets are EMI_GND and GND.

Voltage sources should be attached to these power nets to model voltage regulators. To do this, you must identify the corresponding pins on the voltage regulator module (VRM). For example, in the schematic, Pin5 on U503 connects through an inductor L503 to power net NetL503_1 P1.8V. For Pin14, the net NetL304_1 connects through inductor L304 to power net P1.0V. Later in SIwave you can easily add voltage sources to represent the outputs of the VRM along with the associated series resistance. Ground and the 5-volt power net are supplied off-board through a B-style micro-USB connector with the reference designator P703. Therefore, voltage sources must be added to P703 too.

Similarly, you must identify the power consumers on the board. Typically, RAM, FPGA and microprocessors are the main power consumers. To these ICs, assign current sinks in SIwave. After reviewing the schematic and *"cracking the code"* so to speak, list all the nets and components for assigning current sinks and voltage sources in a table:

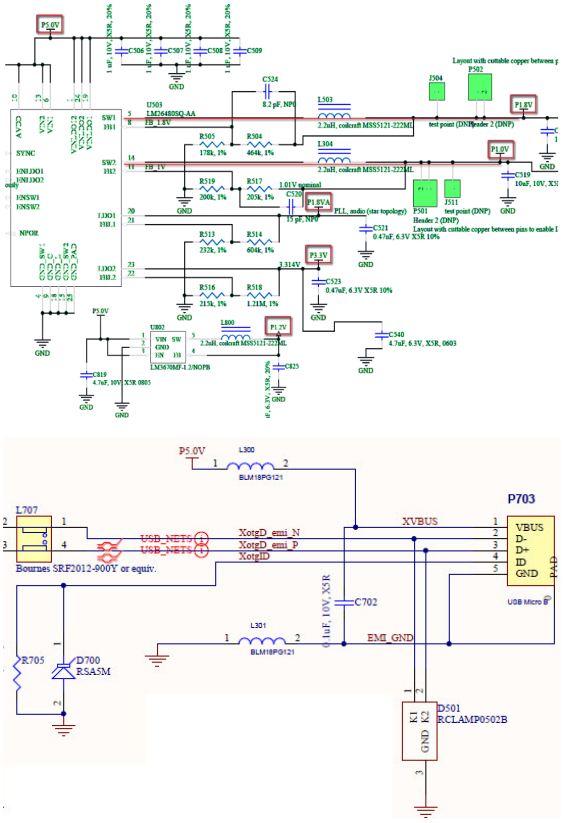

Figure 5. Schematic

Ref. Des	Part Name	Positive Net	Reference Net	Source /Probe	Magnitude
U100	Microprocessor	P3.3 V	GND	Current Source	0.1A
U100	Microprocessor	P1.8V	GND	Current Source	0.1A
U100	Microprocessor	P1.0V	GND	Current Source	0.5A
U201	DDR2 RAM	P1.8V	GND	Current Source	0.2A
U800	FPGA IC	P3.3V	GND	Current Source	0.25A
U800	FPGA IC	P1.2V	GND	Current Source	0.1A
P703	USB_Micro_B	XVBUS	EMI_GND	Voltage Source	5V
U503	Power mgmt. unit	P3.3V	GND	Voltage Source	3.3V
U503	Power mgmt. unit	P1.8VA	GND	Voltage Source	1.8V
U503	Power mgmt. unit	NetL503_1	GND	Voltage Source	1.8V
U503	Power mgmt. unit	NetL304_1	GND	Voltage Source	1V
U802	Buck step down regulator	P1.2V	GND	Voltage Source	1.2V

Stage 3: Power Integrity and DCIR Analyses in SIwave

Using such a table as reference, you can very easily assign current sinks and voltage sources to the board in SIwave before running a DCIR simulation. The SIwave workflow wizard lists all the steps you need to set up a board for simulating its electrical characteristics. For this particular board, you can directly configure the DCIR simulation since most of the steps listed in the wizard occur automatically upon translating the geometry into SIwave using the ODB++ directory. The workflow wizard lets you open the DCIR Configuration window where you can multi-select the components and assign voltage sources to them, all at once. Similarly, assign current sinks. Modify the voltages and currents for these reference designators based on the manufacturer's data sheets. At this point, you can run the simulation to compute DC current and voltage distribution across the board and ICs.

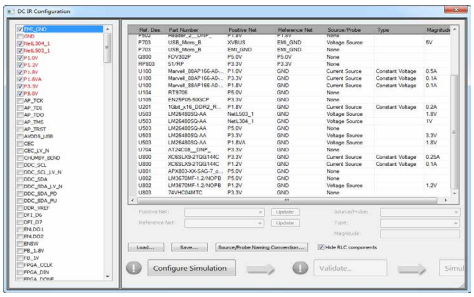

Figure 6. DCIR configuration window in SIwave

SIwave employs an automatic adaptive mesh refinement process that accurately computes the DC voltage drop and current density for the entire board. It also calculates the I^2R-drop and current flow within each element in a PCB model (including resistor, inductor, via, trace, plane, bondwire, source, etc.). The current density plot and the final mesh for our PCB are shown in Figures 8 and 9. SIwave highlights areas of high current density across the board in red. Additionally, you can generate power density and voltage drop plots across the board for all nets. SIwave can analyze DC current distribution return paths. Excessive voltage drop along a line or power delivery network can cause major issues at loads.

Accurate DCIR drop analysis from SIwave is critical for designing optimal power delivery pathways. "What-if" analyses for DC voltage drop, DC currents and DC power losses are possible. Once the problematic areas on the board are found, you can perform "what-if" tests to determine the best approach for improving the layout. The predictive analysis helps you design power delivery networks to efficiently source the power to ICs and minimize power losses. The analysis identifies regions that bear excessive currents and helps you reduce risk of device failure. Adaptive mesh refinement, specifically developed for planar ECAD geometries, is the main reason for generating accurate solutions in SIwave. The overall accuracy of a finite element method (FEM) solver depends upon how accurately a mesh conforms to the design, and of course upon the accuracy of the numerical solution itself. SIwave starts with a high quality initial mesh, which is a collection of triangular elements. Triangles ensure a tighter fit to the geometry and minimize error. A numerical solution's accuracy relies on the density and distribution of mesh elements and the order of the basis functions used within each mesh element. With more adaptive passes, finer granularity ensues progressively from the initial mesh towards the final mesh. Figures 7a, 7b, and 7c show the meshes at various stages of adaptive refinement for a different printed circuit board in SIwave.

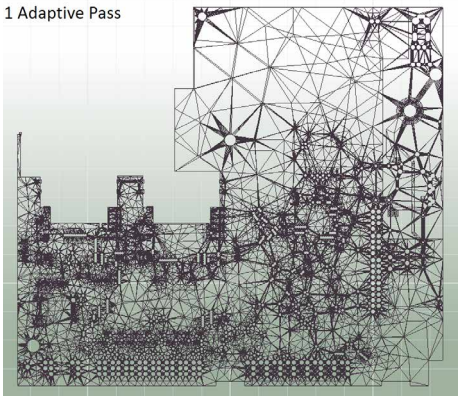

Figure 7a. Meshes due to adaptive refinement after Pass 1 in SIwave

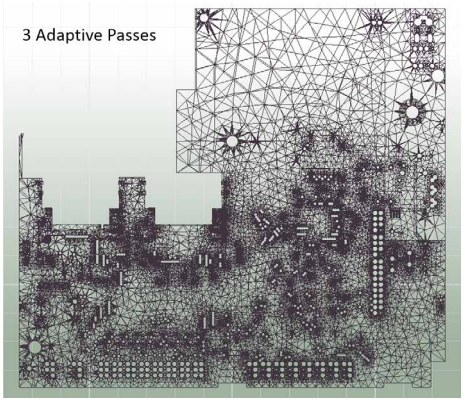

Figure 7b. Adaptive mesh after three passes

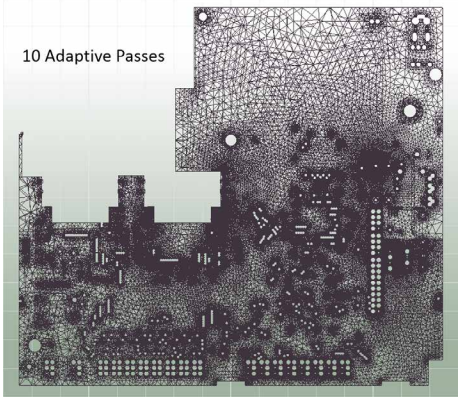

Figure 7c. Final mesh

You cannot tell from the geometry alone where the current is going to concentrate, so the adaptive meshing allows the field solver to determine that and improve its accuracy. More accurate fields translate to more accurate DC resistance values, power dissipation and temperatures.

The adaptive mesh refinement process in SIwave is iterative and based on a convergence criterion that monitors the change in the total power loss from one adaptive pass to the next. So, in each pass, the solver computes the total Ohmic power loss and compares it to the power loss in the previous pass. The difference is converted to a percentage and compared with the user-specified error tolerance. If it is smaller than the specified value, the solution is deemed to have reached convergence.

This automated adaptive refinement technique guarantees an accurate solution with the fastest speed and minimum use of computational resources. To give you a sense of how fast our board is solved in SIwave, the DCIR simulation of our PCB converges in just 30 seconds.

Note: For a quick thermal analysis, without detailed CFD modeling in Icepak, you can export the Joule power losses in the metal directly from SIwave to Ansys Mechanical. This type of analysis does not consider the power losses of attached circuit components, such as ICs and resistors. In this case Ansys Mechanical computes a solution to the heat conduction equations in the board using a simplified convection boundary condition at the exterior surfaces of the board. We recommend using our reference design flow when the greatest accuracy is required as it incorporates CFD analysis in Icepak from where the resulting temperatures are transferred to the board in Mechanical as well as for the components and the heat sinks.

For the purposes of the multiphysics problem of this PCB, the authors considered the board as well as all the components (plus the heat sinks) in the analysis. We will configure a CFD analysis of the board and the ICs by coupling SIwave and Icepak in the next stage of our reference design flow.

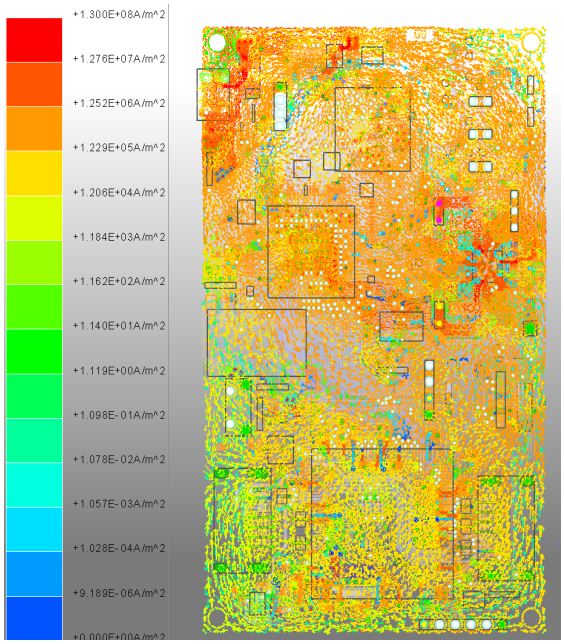

Figure 8. Current density plot

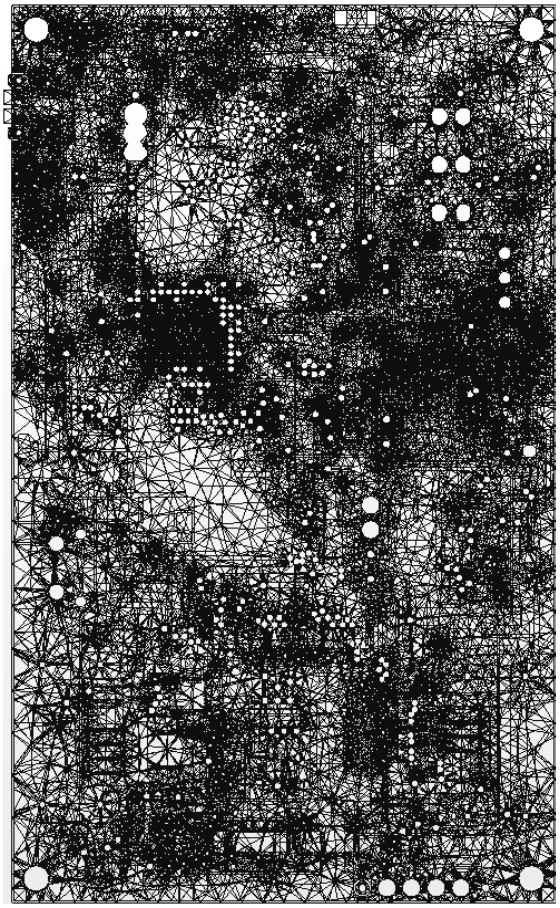
Figure 9. Final mesh of the PCB

Stage 4: Automated and Iterative Thermal Analysis

Based on the DCIR analysis, SIwave also generates Icepak power maps for the board. The I^2R power losses from SIwave serve as the starting point for the thermal analysis.

During the Icepak Simulation Setup in SIwave, you can define the worst-case thermal design power for each component. The power dissipation values come from the manufacturer's data sheets. Enter these values for the ICs and voltage regulators. Optionally, include heat sinks for these components. Then choose the type of thermal simulation: forced convection or natural convection (still air). For our board, both types of thermal analyses were performed.

When you launch this simulation, it invokes the Icepak solver directly from SIwave. The Icepak solver is launched in non-graphical mode. The PCB design and setup information gets transferred into Icepak along with DC power loss maps from the SIwave analysis. The Icepak analysis calculates the heat flow and temperatures across the board and for all the objects that were included in the simulation. For convenience, basic thermal analysis results can be displayed on SIwave as shown by the thermal data plots in Figure 11. On our board, hot spots develop around voltage regulators, and the temperature near the microprocessor increases.

Stage 5. Temperature Post-processing in Ansys Icepak

SIwave lets you directly open the PCB design in Icepak where you can perform detailed post-processing operations on the board that exceed that shown above. Within Icepak, a report (see Figure 12) can be generated listing temperatures for the board and all the desired objects, along with the user-entered operating temperature limits from the manufacturer's datasheet. The report lets you confirm whether the board and objects are within the temperature limits. Components lying beyond these temperature limits are prone to damage. You can even specify arbitrary temperature limits. Objects that are above these limits will be flagged in red; marginal cases, where temperatures are within 5 percent of the safe operating limits, will be flagged in orange.

You can also produce temperature maps for all the objects and the board as shown in Figure 13 for a natural convection (still air) thermal simulation. Heat sinks are added based on the selections in SIwave.

Contour plots on a cut plane can also be generated in Icepak for the board and its components. In our board, these plots show that the heat is propagated downstream by the air flow away from the hottest components (see Figure 14).

Additionally, Icepak lets you generate particle traces and vector plots (see Figure 15). Particle traces represent the path of hypothetical massless particles through the model. This path is calculated based on the computed flow field. Vector plots indicate the direction and speed of the air flow. Arrows in orange and red represent the fastest air flows. The length and direction of the vector represent the magnitude and direction of the velocity at a specific location in the PCB model.

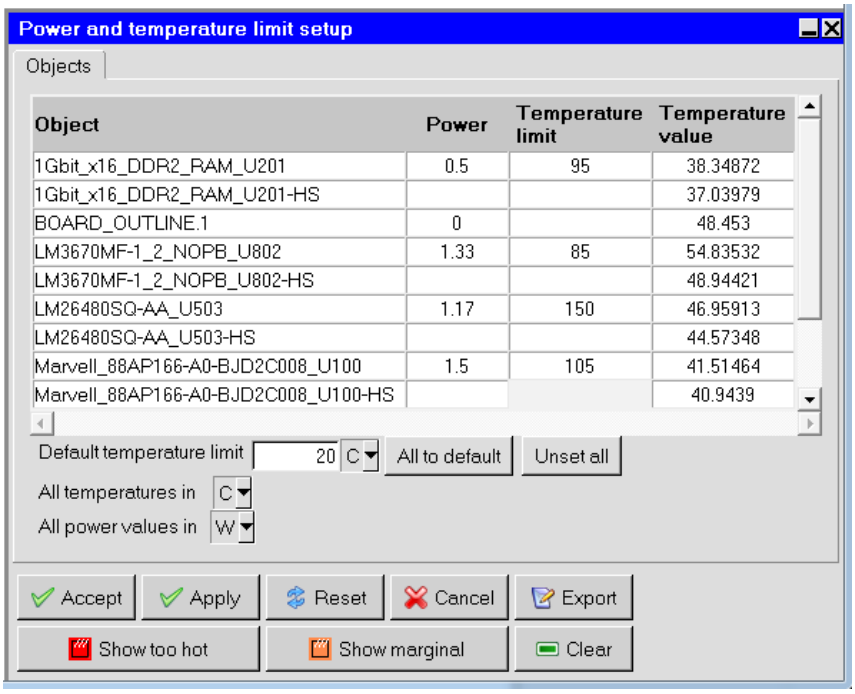

Figure 12. Report dialog in Icepak

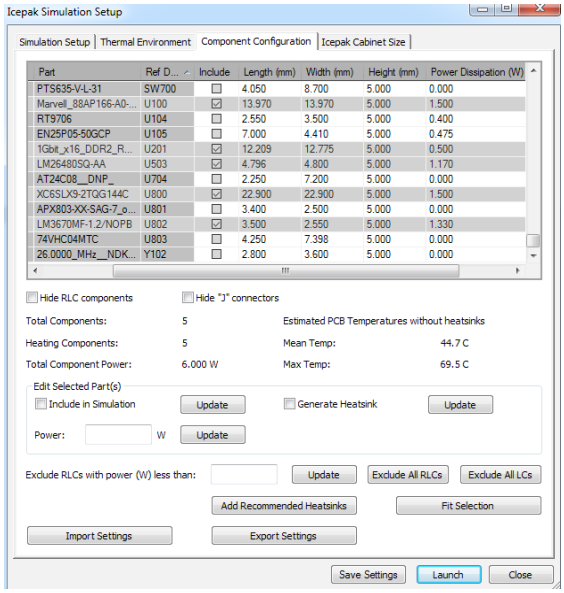

Figure 10. Icepak simulation setup in SIwave

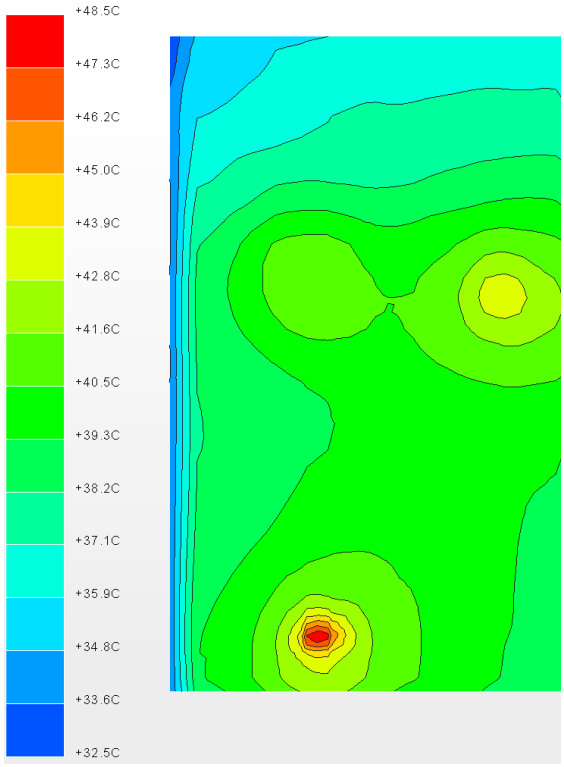

Figure 11. Thermal hot spots in SIwave

Stage 6: Generate Temperature Profiles for the Board in Icepak

The power dissipated within the PCB planes and traces defines Joule heating. This can impact the board adversely by introducing mechanical reliability issues. Because temperature variation across the board gives rise to structural problems, it makes sense to generate a temperature profile for the board and its components in Icepak from the CFD solution. Soon in this design flow, you will see that this temperature profile can easily be incorporated into the Ansys Mechanical calculations for thermal stress, deformation and elastic strain on the board.

Generating the temperature profile from Icepak is very easy. The CFD Post/Mechanical Data menu option in Icepak writes out a file with the temperatures for the entire board and the ICs that were included in the thermal simulation. This file comes with a .loads extension. This temperature file acts as a thermal load within Mechanical during the structural stress analyses. A sample data set from the .loads file is shown in Figure 16. The columns represent the x, y and z coordinates with temperatures defined in Kelvin.

The CFD Post/Mechanical data writes out this LOADS file in the SIwave and Icepak results folder.

Stage 7: PCB Preparation for Use in Ansys Mechanical

Localized temperature increases cause thermal expansion and stress that can significantly reduce product reliability. Before we perform the structural analysis, we need to prepare the PCB in Ansys SpaceClaim Direct Modeler (SCDM). The PCB is imported into SCDM where it is prepped with the heat sinks and component outlines needed for our structural analysis. These heat sinks can be exported as .step files from Icepak.

This technique for preparing the geometry is used because it is convenient to first develop a simplified layout topology version of the board separately since a true 3-D ECAD model in acis is undesirable due to performance limitations. The ECAD data will be imported later during the trace mapping step. Best practices show that mapping the ECAD data with a hexahedral mesh provides the best performance and accuracy, while meshing the heat sinks using a tetrahedral mesh provides the greatest accuracy within Ansys Mechanical.

Preparing this MCAD geometry is accomplished very easily within SCDM. The ODB++ directory of the board was archived in the form of a .tgz file by Altium Designer. A simple drag & drop operation of the .tgz file translates it into SCDM 3-D interface. The exported file from Icepak that contains all the heat sinks is then imported into SCDM for placement on the PCB. The heat sinks are combined in SCDM and will be treated as solid objects in Mechanical.

The 3-D SCDM file (of the PCB and the corresponding heat sinks) eventually gets imported into Mechanical through the Ansys Workbench platform.

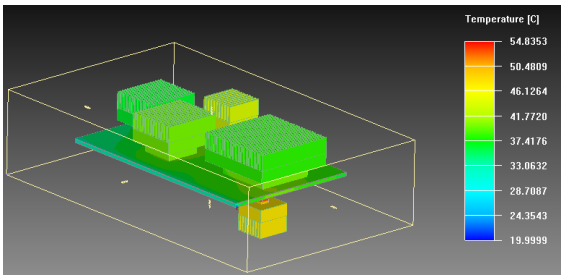

Figure 13. Temperature map

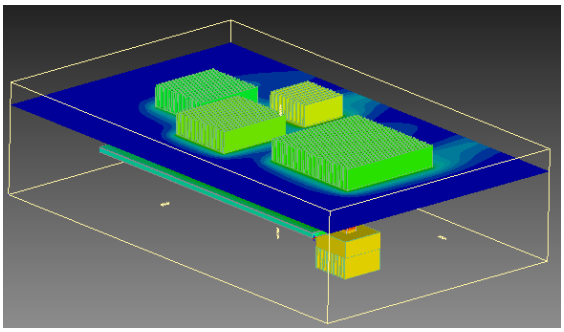

Figure 14. Contour plot

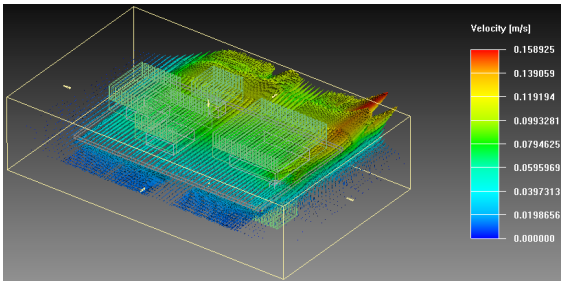

Figure 15. Vector plot

```
BODY "Marvell_88AP166-A0-BJD2C008_U100"
0.011274 0.052012 0.005584 314.255280
0.011274 0.052012 0.006067 314.192505
0.011274 0.052012 0.006550 314.069305
0.011274 0.052158 0.005584 314.254120
0.011274 0.052158 0.006067 314.191650
0.011274 0.052158 0.006550 314.072235
0.011274 0.052523 0.006550 314.073853
0.011274 0.052773 0.005584 314.257507
0.011274 0.052773 0.006067 314.194977
0.011274 0.052773 0.006550 314.075531
0.011274 0.053023 0.005584 314.259003
```

X Y Z Kelvin

Figure 16. Sample data set from. loads file

Stage 8: Assemble the Project in Ansys Workbench

Ansys tools offer a lot of freedom in the order in which you can generate the temperature profile from Icepak, prepare the geometrical model in SCDM and generate the ECAD data file. They also give you flexibility regarding how these "subsystems" are applied to the PCB in Mechanical for multiphysics analysis. This multiphysics analysis is made possible by using Ansys Workbench, a framework for assembling all the subsystems and linking the temperatures and the ECAD data onto the board in Mechanical. Build the project in Workbench as shown in Figure 17 — the Icepak subsystem in the figure points to the .loads file that contains all the temperature data for the board, components and heat sinks. The External Data component subsystem points to the original .tgz file of the ODB++ directory. The Geometry cell in the Static Structural subsystem is used to import the model in Mechanical from SCDM. Each time you use the Edit cell of the model, Workbench re-reads the upstream data and accordingly updates the project in Mechanical.

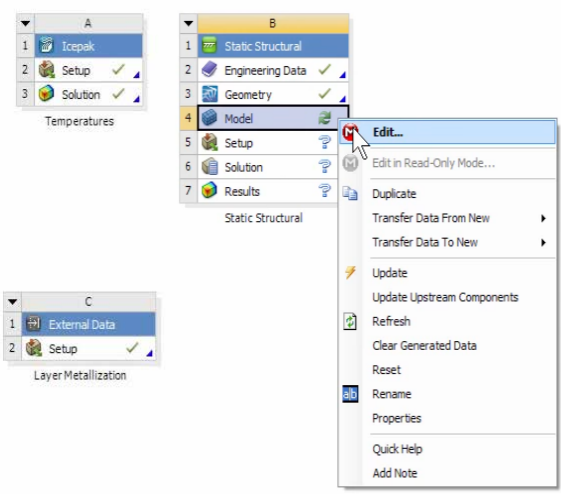

Figure 17. Project in Workbench

Once the board is imported into Mechanical, ensure that there are as many contacts as there are heat sinks. Gather the required materials from the Engineering Data cell; in this case, we add Aluminum Alloy 6061, Copper Alloy and FR4. In Mechanical, the heat sinks are assigned Aluminum Alloy 6061 and the PCB layers are assigned FR4 as their material property. To assign copper for the stackup layers, we need a mesh. This is because we need to know the proportion of metal to non-metal on each layer of the PCB for mapping the layer metallization (ECAD trace) data to the board (which happens by linking the board in Mechanical to the archived .tgz file after generating a mesh).

Stage 9: Import Layer Metallization on PCB with "Trace Mapping Technique"

Ansys Mechanical produces a uniform mesh of hexahedral elements in the board. All the 3-D objects (ICs and components) and heat sinks are represented by a tetrahedral mesh. However, the board is meshed with hexahedral elements to exploit Ansys Mechanical's metal fraction assignment technique as it works best with a hex mesh. After generating the mesh, material for the metal fraction on each layer is defined as copper. The cross-section of the PCB is also automatically taken into account for calculating the metal fraction.

In the metal fraction assignment technique, Mechanical automatically computes the effective material properties on an MCAD mesh based on the spatial distribution of metal and dielectric in the ECAD model.1 In this technique, Ansys Mechanical generates a point cloud representation of the internal details of the entire board on a rectangular grid. Each cell is divided into sampling points, which represent a mixture of metal and dielectric materials. They are assigned onto the finite element mesh as data points. Using these data points, Mechanical assigns an effective material property to each mesh element by computing *a weighted average* of the metal and dielectric. As it assigns the property from element to element, this eventually develops into a spatially varying metal fraction on a large scale. This metal fraction can be actually seen once it's imported onto the mesh. A metal fraction of 1 means the element is all metal. A metal fraction of 0.5 means the element is half metal and half dielectric.

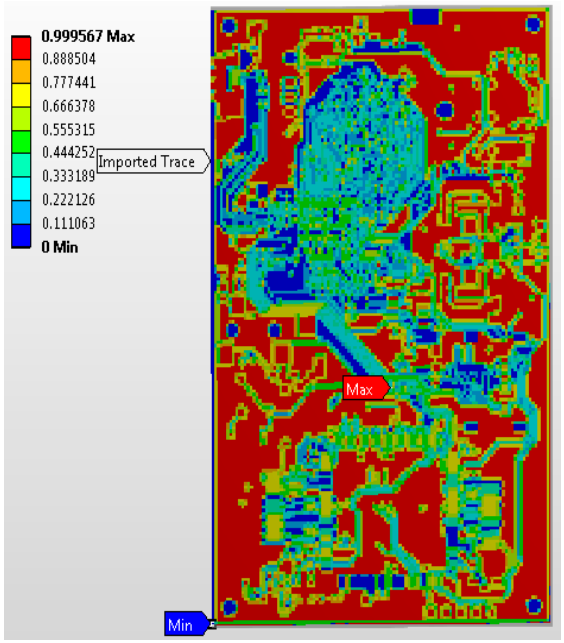

Figure 18. Imported layer metal without heat sinks

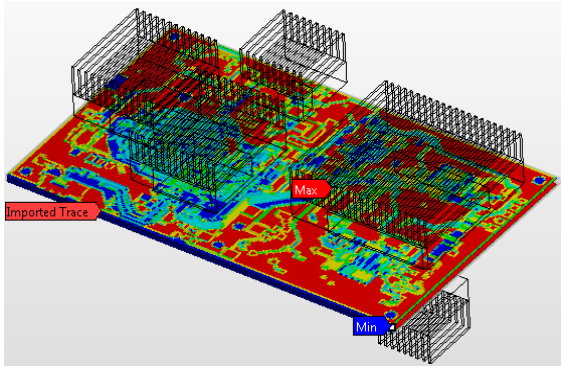

Figure 19. Imported layer metal with heat sinks

When using actual geometry for traces and vias, computing the thermal induced stress is a daunting task due to the enormous geometrical complexity of ECAD data. This combination of hexahedral mesh with trace mapped metal fraction for the board and tetrahedral mesh with homogenous material for the objects and heat sinks is well-suited for performing structural simulation of ECAD in Mechanical. This is enabled by forming 3-D layered solid parts and mapping the layer metallization data onto the finite element mesh. The imported trace metal on the board is shown in Figure 18. Metal fractions on the board with and without heat sinks are shown in Figures 18 and 19.

Regions in red represent higher copper density while those in blue are considered to be dielectrics.

Stage 10: Transfer Temperatures from Icepak to the Board in Mechanical

Essentially, at this point we can transfer temperatures for the entire board as well as its components and heat sinks. Ansys Mechanical also allows you to choose exclusively only those objects of interest for which you want temperatures to be transferred through the built-in Icepak subsystem within Workbench. However, in our multiphysics problem, we included all the components and their heat sinks, as well as the board. The temperatures for the entire board and all its components and heat sinks are contained in the .loads file written out from Icepak. By way of this .loads file, all the temperature values are mapped onto the geometry in Mechanical.

Figure 20 shows the temperature map once applied on the model in Mechanical. This temperature map is due to the natural convection (still air) thermal co-analysis from within SIwave and Icepak. So, in this way, the temperature field from the CFD analysis is applied on the model. See the temperature field mapped onto the board in Mechanical in Figure 20.

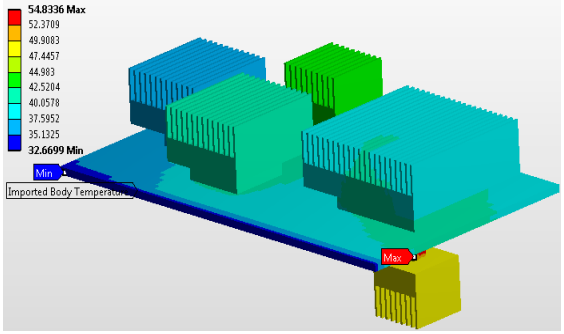

Figure 20. Icepak temperatures mapped onto the board in Mechanical

Stage 11: Simulate the Board for Thermal Stress, Deformation and Elastic Strain

The heat generated by ICs and calculated from Joule heating will cause structural deformation. Equivalent stress, deformation and elastic strain due to Joule heating computed in Icepak, induced by the power loss in SIwave, can now be easily analyzed for the entire model in Mechanical. Shown below are figures illustrating the stress and deformation (exaggerated for visualization purposes) for the PCB model. Observe that the board tends to bow downward. Recall the principle of the bimetallic strip — a higher concentration of copper on the top layer causes the board to bow downward due to copper's higher coefficient of thermal expansion compared to FR4. See Figures 21 and 22 for the mechanical model solution producing warping shown by the deformation contours. Stress contours for the overall models are also shown.

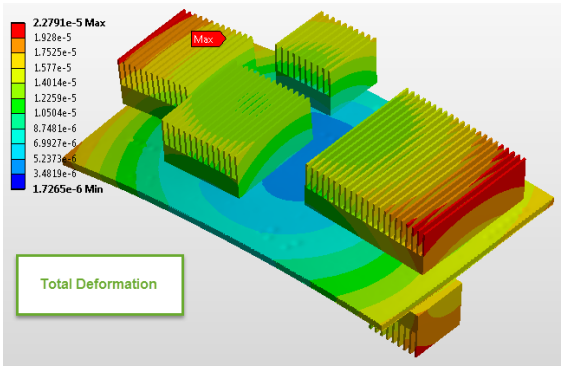

Figure 21. Thermal-induced deformation in Mechanical

The elastic strain plot (Figure 23) helps us determine possible locations of delamination and fracture. For our board, maximum strain is under the microprocessor U100; the region is depicted by the max marker. This is where the IC may tend to pull away from the PCB. The heat sink along with the IC is treated as one lumped metal of aluminum which is fastened to the PCB underneath it. The PCB has two different materials (copper and FR4), which give rise to the high strain shown in the Figure 24. This is an approximation in which we have simplified the interface between the package and the board — the interface in actuality is achieved by solder balls and bumps. For this simplified analysis we used a basic cuboid to model the IC, and assigned it the same material (aluminum) as the heat sink.

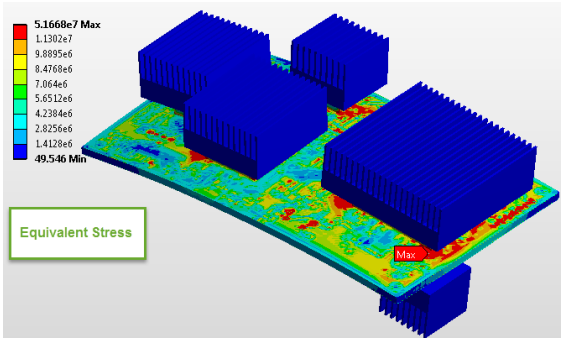

Figure 22. Thermal-induced stress

Conclusion

In reality the IC package has a more complicated shape made of plastic or ceramic, and is connected to the board with solder balls. You could perform a more detailed analysis including more realistic package geometry and materials along with models of the solder balls to further assess the robustness of the board. One possible way to perform a more detailed analysis would be to utilize sub modeling. This will help you understand whether the board might fail with additional results analyses, such as fatigue and fracture processing. For example, Ansys solutions can simulate the influence and underlying physics of the flip-chip attachment process commonly used in the semiconductor industry; after the process is complete the IC assembly is subjected to thermal cycling to assess the cumulative damage in individual components. Stress, strain and deformation due to CTE mismatch can be determined at both the component and assembly level for solder bumps, solder balls, die, underfill and for the PCB.

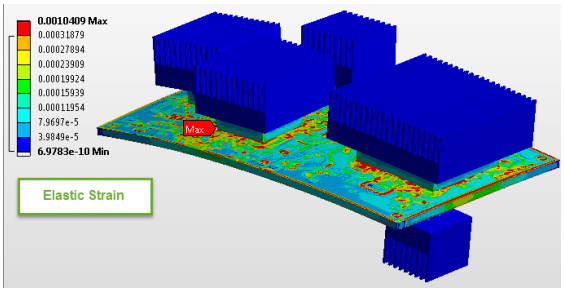

Figure 23. Elastic strain

Our reference design flow can help you solve multiphysics DC thermal and structural problems of any electronic product using Ansys tools. You can do all of this analysis by using Ansys products within a single framework wherein each product is tailored to solve a particular problem. By taking advantage of all the features and strengths of each Ansys product, you can combine them to create a multiphysics solution for all the electrical, thermal and mechanical problems of a PCB.

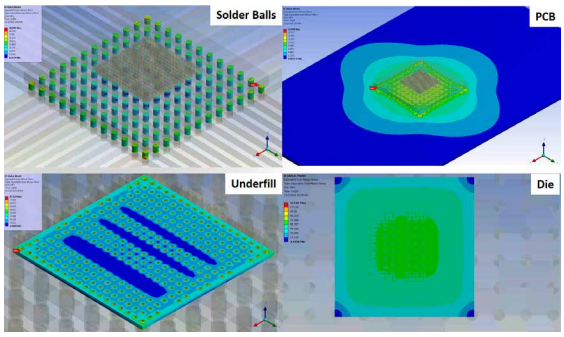

Figure 24. PCB Flip Chip Attachment Process and Thermal Cycling to Assess Cumulative Damage in Components

References

[1] G. Refai-Ahmed, H. Shi, M. Keshavamurthy, S. Shah, D. Ostergaard, B. Boots, T. Pawlak, & S.G. Pytel; "Electronic PCB & Package Thermal Stress Analysis"; *IEEE Electronics Components and Technology Conference*, May 31-June3, 2016.

Additional Reading

S.G. Pytel, L. Williams, M. Raju; "Package and Board Power Integrity Design with Ansys SIwave-PI"
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